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MODEL 1

FUNCTIONAL CHARACTERISTICS

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Preface

This reference manual for functional characteristics is designed as a companion volume to the operating procedures for the OMEGA computer (publication number 22291360).

The manual describes the OMEGA features and advantages. The contents are organized to acquaint the reader with the OMEGA basic output structure. For a detailed description of OMEGA see:

- OMEGA Maintenance Manual, Volume 1 - publication number 22291361
- OMEGA Maintenance Manual, Volume 3 - publication number 22291363

The reader is assumed to have a working knowledge of IBM System/370 Principles of Operation, GA22-7000. In addition the reader should have familiarity with programming System/360 or System/370 models.

This manual is divided into sections as follows:

CONSOLE FILE - Functions of this microprogram-loading device.

CONSOLE PRINTER-KEYBOARD - Programming and configuration information for the printer-keyboard units.

FEATURES DESCRIPTIONS - A description of major system features such as OS/DOS compatibility, the interval timer, and the time-of-day clock.

EXTENDED CONTROL - A description of the following features: the extended control feature, including a description of the extended control PSW, store status, program event recording, dynamic address translation, channel indirect data address, and clock comparator and CPU timer.

INPUT/OUTPUT CHANNEL CHARACTERISTICS - Information about the byte-multiplexer, and block-multiplexer channels.

SYSTEM CONFIGURATION - A list of standard and available feature dependencies.

SYSTEM TIMING - Detailed timings for internal CPU functions (instruction execution), the printer-keyboard, the byte-multiplexer channel, and the block-multiplexer channels.

Contents

FIGURES

TABLES

SECTION 1

INTRODUCTION

Section 1. Introduction

OVERVIEW

OMEGA is a high-availability general-purpose data processing system that offers significant price/performance improvements over an IBM System/370 Model 145. It provides the reliability, availability, performance, and convenience demanded by both business and scientific users. The various CPU and I/O configurations allow tailoring computing facilities to match your company's growth.

Each CPU cycle requires 50 nanoseconds. The times required for instruction execution are given in the timings section (section 6) of this manual.

The block-multiplexer channels are capable of handling an aggregate data rate of about 5 million bytes per second with the standard double-word buffer feature installed.

The maximum byte-multiplexer channel data rates are 50,000 bytes per second in byte mode and 180,000 bytes per second in burst mode. Most input/output devices that can be attached to IBM System/360 and System/370 can be attached to this system.

This publication is intended as a reference for users of OMEGA; only items that are unique to OMEGA are discussed in detail. For this reason, a comprehensive understanding of the information in the IBM System/370 Principles of Operation, GA22-7000, is necessary for effective use of this publication.

Several programming support systems are available for use with OMEGA. These include the operating system (OS/VS1), the disk operating system (DOS/VS), and VM/370. Refer to the IBM System/360 and System/370 Bibliography, GA22-6822, for abstracts of IBM programming publications that apply to these systems.

STANDARD FEATURES

The main storage capacities (253,952 to 2,088,960 bytes), channel configuration, and other system specifications are given in the OMEGA system configurator section. OMEGA incorporates the following facilities as standard. These facilities are described in other sections of this manual and in the IBM System/370 Principles of Operation, GA22-7000.

- Advanced Control Program Support
- Audible Alarm
- Block-Multiplexer Channels 1 and 2
- Byte-Multiplexer Channel
- Byte-Oriented Operand
- Channel Indirect Data Address
- Channel Retry Information
- Conditional Swapping

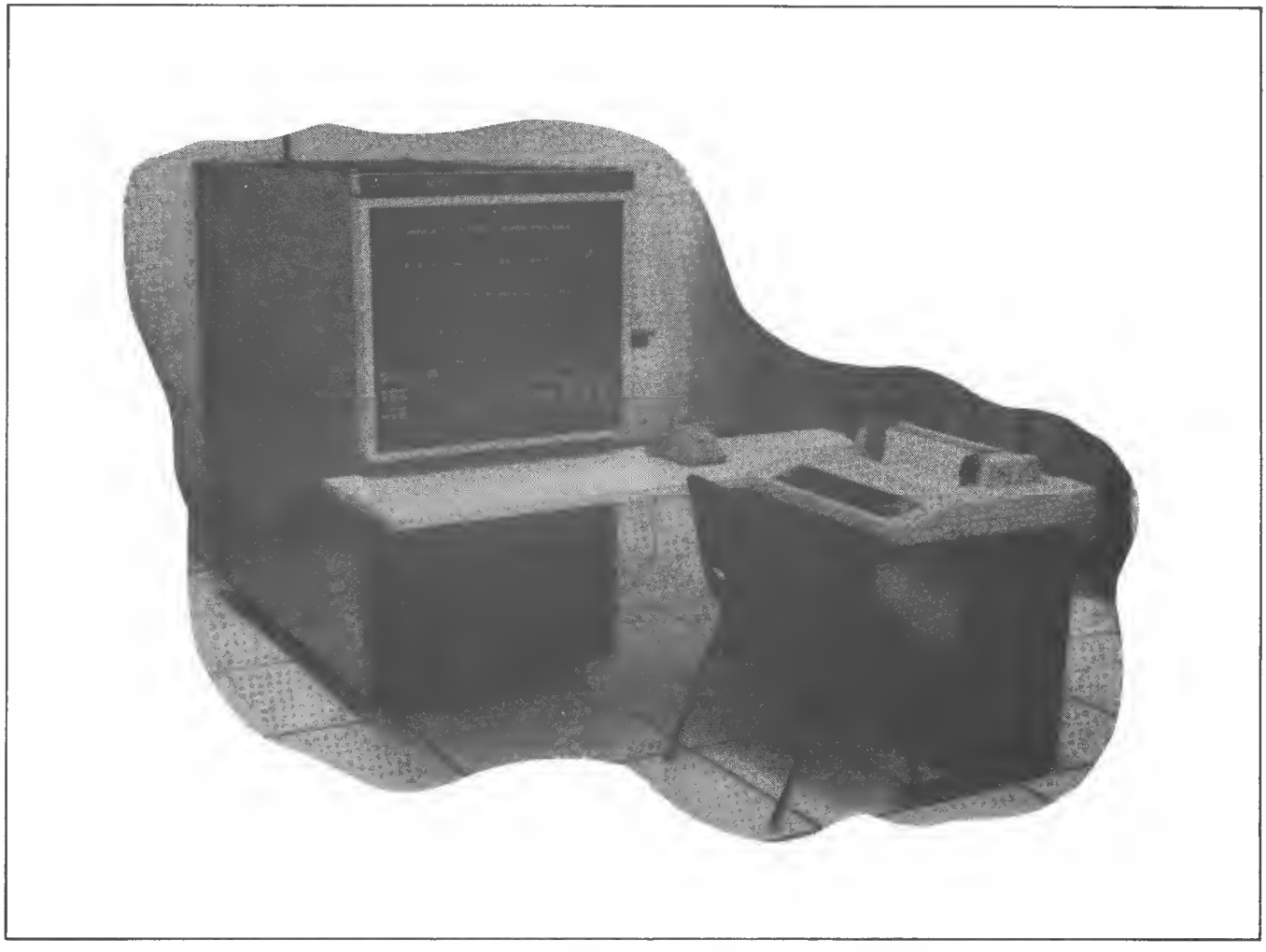

Figure 1-1. OMEGA Data Processing System

- Console File
- Control Registers
- Dynamic Address Translation
- Error Checking and Correction (ECC)
- Extended Control
- Floating-Point (includes extended precision) and System/370 Floating-Point Instruction Set
- Interval Timer
- Machine-Check Handling
- Microprogram Instruction Retry
- OS/DOS Compatibility
- Program-Event Recording
- Storage Protection (Store and Fetch)
- Time-of-Day Clock
- System/370 Commercial Instruction Set (includes all standard and decimal instructions listed in the IBM System/370 Principles of Operation, GA22-7000, except that the store channel ID instruction cannot set condition codes 1 and 2)
- Virtual Machine Assist
- Double Word Buffer (Block-Multiplexer Channels)
- Clock Comparator and CPU Timer
- Console Printer-Keyboard
- 12K (Words) Control Storage

OPTIONAL FEATURES

The following features are optional. For more information, refer to section 5, OMEGA System Configuration.

- Block-Multiplexer Channels 3 and 4
- Main Storage Over 1 Megabyte to 2 Megabytes
- Additional 4K (Words), Total 16K, Control Storage

DATA REPRESENTATION

This system is both character and word oriented; the basic addressable unit is an 8-bit byte (a character, two decimal digits, or eight binary bits). This provides more efficient use of storage, high effective input/output rates for decimal data, variable field length, broad and flexible code conversion, decimal arithmetic, 32-bit words and 16-bit halfwords for fixed-point arithmetic, 32-bit words and 64-bit doublewords for floating-point arithmetic, and powerful instructions for such functions as translate and edit.

COMPATIBILITY

Within the storage capacity, internal and input/output channel processing rates, and type of input/output devices that can be attached, compatibility is maintained with IBM System/370 and System/360 models, with the following exceptions:

- Programs using machine-dependent data (for example, machine logouts).
- Programs using the ASCII bit (PSW bit 12).
- Programs that depend on features of I/O devices that are not implemented on this system.
- Programs that use main storage locations between address 128 and 736 (decimal) after a diagnostic logout into program storage. However, such programs may be executed if main-storage locations that are overlaid by the diagnostic logout are restored with the program requirements followed by an appropriate program restart procedure.

Any attempt to continue processing after a diagnostic logout to main storage without restoring the program information to the logout area will have unpredictable results.

The 736-byte extend (the permanently assigned main storage locations) can be reduced to 512 bytes by moving the 224 bytes between locations 512 and 736 into another main-storage area. The technique used to accomplish this relocation depends on the application.

SYSTEM RESIDENCE AND MAINTENANCE-STORAGE REQUIREMENTS

Optimum performance and maximum system availability are maintained when a disk-storage facility (DSF) is provided for residence of the operating system and the application-program files, storage of diagnostic tests, and storage for error-logout information. In the remainder of this manual, these storage requirements are assumed to be a disk storage facility attached through a block-multiplexer channel. For this reason, block multiplexer channel 1 with a DSF is listed as a selective feature required for minimum system configuration.

SYSTEM UNITS

The OMEGA system consists of the central processing unit, storage control unit, main storage, the system console, and other facilities necessary to perform arithmetic

functions and logical processing of data. The system also contains input/output channel circuitry for control of data transfers between storage and I/O devices.

Control Storage

Up to 16K words of control storage are housed in the CPU. Control storage contains the microprogram upon which all system operations depend. Once loaded from the disk, control storage is not available to the user and should not be modified. To do so can make application results unpredictable.

Main Storage

Main storage can contain up to 2048K bytes. Application-program data is read out of (or into) main storage eight bytes (a doubleword) at a time increasing system performance.

Error checking and correction (ECC) on main storage provides automatic single-bit error detection and correction. It also detects all double-bit and most multiple-bit storage errors but does not correct them. Parity checking is used to verify other data in the system that is not contained in main storage.

Main storage addressing begins at location 0 and continues up through the highest installed main storage byte location. Fixed main storage allocations for all configurations ensure compatibility between OMEGA and IBM System/370. Table 1-1 shows the fixed main storage allocations.

Table 1-1. Fixed Main Storage Allocations

Decimal Word Address	Length in Words	Purpose
0	2	Initial program-loading PSW (also restart new PSW)
8	2	Initial program-loading CCW1 (also restart old PSW)
16	2	Initial program-loading CCW2
24	2	External old PSW
32	2	Supervisor-call old PSW
40	2	Program old PSW
48	2	Machine-check old PSW
56	2	Input/output old PSW
64	2	Channel status word
72	1	Channel address word
76	1	----------
80	1	Timer
84	1	----------
88	2	External new PSW
96	2	Supervisor-call new PSW

Table 1-1. Fixed Main Storage Allocations (cont)

Decimal Word Address	Length in Words	Purpose
104	2	Program new PSW
112	2	Machine-check new PSW
120	2	Input/output new PSW
128	8	Reserved
160	8	I/O communications area
192	10	Reserved
232	2	Machine-check interruption code
240	2	Reserved
248-736	122	Diagnostic logout area

The highest 8K bytes of main storage are reserved for UCW's. The remaining byte locations of main storage are available for programming functions.

Local Storage

Local storage is a facility that is used to contain working areas for high-speed access by the arithmetic/logic unit and other data-flow components. Certain areas of local storage are reserved for:

- General registers 0 through 15
- Floating-point registers 0, 2, 4, and 6
- Instruction counter
- Control registers 0 through 15

Displaying or altering local-storage areas are discussed in the OMEGA Operating Guide, publication number 22291360.

Microprogram Loading

Microprogram control words are loaded from read-only magnetically encoded disks that are read by the console file. These disks are prepared for each configuration and shipped with the system. Additional disks contain a comprehensive set of system diagnostics that are used to assist in locating a failing component. The actual initial microprogram load (IMPL) procedures, as well as the other operator instructions, are included in the OMEGA Operating Guide, publication number 22291360.

After the microprogram is loaded into control storage, system operation can be initiated by the operator from the system control panel. Depending upon the job requirements and the operating system being used, the microprogram sequences control further system operations.

For additional information, refer to the sections on console file and control storage requirements.

ERROR HANDLING

If application-program errors occur (such as illogical action request), the operating system attempts to handle the exception and provides any necessary operator messages. Refer to the applicable programming publications for the IBM operating system being used. These are listed in the IBM System/360 and System/370 Bibliography, GA22-6822.

If a failure occurs within the system or an I/O unit, provisions are made to retry the failing operation. Error-logout facilities are incorporated to record any such failures. (This is in addition to any provisions made by the operating system for error logging.)

Microprogram instruction retry, limited channel logout, storage validation (error checking and correction-ECC) for main storage, and other error-detection and error-handling provisions are standard.

Microprogram Instruction Retry

The ability to recover from most intermittent failures is provided by retry techniques. CPU retry is done by microprogram routines. When an error is detected, before the source data is altered, a microprogram routine returns the CPU to the beginning of the operation (or to a point during the operation that was executed correctly), and the operation is repeated up to four times.

Error Checking and Correction (ECC)

Error checking and correction circuitry for main storage automatically corrects single-bit errors. Automatic detection of double-bit errors is also provided.

Channel Retry Information

Channel retry information is provided in the extended channel status word (ECSW). This information may be used with channel check handler (CCH) routines in the retry of failing I/O operations. Where possible, channel microprogram instructions are retried using the existing CPU-retry machine logic. When an uncorrectable channel-CPU error occurs, the channel affected by the error provides a channel status word (CSW) and an extended channel status word (ECSW). The affected channel also provides a logout via an interruption or a condition code 1 setting store operation.

Command Retry

Command retry is a control-unit-initiated procedure between the channel and the control unit (not all control units have this capability). No I/O interruption is required. The number of retries is device dependent.

ATTACHED I/O DEVICES

The following two I/O devices are attached directly to the CPU through integrated adapters. These are described in detail in other sections of this manual. In addition, a wide variety of input/output devices can be attached through the input/output channels.

- Console file

  This device is used to load control storage with either the normal microprogram or with diagnostic microprograms.

- Console printer-keyboard

  This unit serves as the on-line input/output device for operator/system communication. It is used to enter or display programming-systems control parameters and responses to system messages. In addition it can display or alter application data.

INPUT/OUTPUT CHANNELS

This section is an introduction to the input/output channels. Refer to the section on input/output channel characteristics for detailed information.

The byte-multiplexer and block-multiplexer channel operate with the same I/O instructions and command formats used for IBM System/370 models and for IBM System/360 models 25 and up. Block-multiplexer channels operate with attached I/O control units by using signal sequences defined in IBM System/360 and System/370 I/O Interface - Channel to Control Unit Original Equipment Manufacturers Information, GA22-6974. Block multiplexer mode, and additional tag lines (data-in, data-out, mark 0-in, and disconnect-in) are described in the input/output channel characteristics section.

The byte-multiplexer channel has 256 unshared subchannels and is available to address up to 256 devices.

With each block-multiplexer channel, up to 256 I/O devices can be addressed. Each block-multiplexer channel is dynamically assigned unit control words (UCW's) from a pool. The number allocated per channel is flexible and may be varied from job to job. The size of the pool is 432 unshared UCW's and 16 shared UCW's.

Channel Interface

A standard input/output interface is provided for attachment of a wide range of I/O devices. This interface is a set of standard electrical connections through which data and control signals are exchanged between the CPU and attached I/O devices.

For block-multiplexer channel operation, the standard interface is extended to include the data-in, data-out, mark 0-in, and disconnect-in lines.

Data-in/data-out, used with service-in/service-out, permits data transfers to take place faster than using only the service-in/service-out tags. These facilities can

also be utilized to permit the placement of a control unit at a greater distance from the channel.

Mark 0-in is used in the interface sequence when a control unit signals a command retry.

Disconnect-in provides control units with the ability to alert the system for a malfunction that prevents the control unit from signaling properly over the input/output interface.

Byte-Multiplexer Channel

One byte-multiplexer channel is included as part of the basic system. The channel data rate is 50,000 bytes per second. This data rate allows for typical interface delays but does not include block-multiplexer channel interference. The byte-multiplexer channel normally operates in byte mode. In this mode, the single data path of the channel can be timeshared by a number of low-speed I/O devices operating simultaneously. The channel, on demand, handles data to or from these devices (one device at a time) in groups of bytes as determined and specified by the device being serviced. Such interleaved segments of information can consist of a single byte, several bytes, or status or control information used to initiate a new sequence.

Certain I/O devices may force the byte-multiplexer channel to operate in burst mode. The burst can consist of a few bytes, a whole block of data, or a sequence of data blocks with associated control and status information. The data rate in burst mode is 180,000 bytes per second. This data rate allows for typical interface delays but does not include block-multiplexer channel interference.

Block-Multiplexer Channel

Up to four block-multiplexing channels are available. This type of channel is optimized for relatively high-speed burst operations and is designed to multiplex complete blocks of data, permitting the device to disconnect only after channel end or upon execution of a halt I/O or halt device instruction.

The multiplexing facility of the block-multiplexer channel allows the interleaved execution of several channel programs by the same channel.

Block-multiplexing control (defined in the IBM System/370 Principles of Operation) allows operation of the block-multiplexer channel as a selector channel.

Attachable Input/Output Devices

I/O devices that can be attached to OMEGA are as listed in the IBM System/370 Input/Output Configurator, GA22-7002, except those requiring direct control.

SECTION 2

CONSOLE

Section 2. Console

CONSOLE FILE

The console file is the initial microprogram loading (IMPL) device for the system. It provides, on removable disks, all microprograms for the system. Each disk contains a full control-storage load of system microcode customized for each individual system configuration. The several disks supplied with the system supply the microprograms required for System/370 operation, emulators, diagnostics, etc., to be loaded into control storage.

Power to the file is normally off. An IMPL (automatic with power on) or diagnostic operation initiated from the system console turns console-file power on, and loading of data from the file occurs. Power to the console file is turned off automatically when loading is complete.

The console file is located under the operator's console table. Room to store a number of disks is provided inside the cover. The console file is shown in figure 2-1.

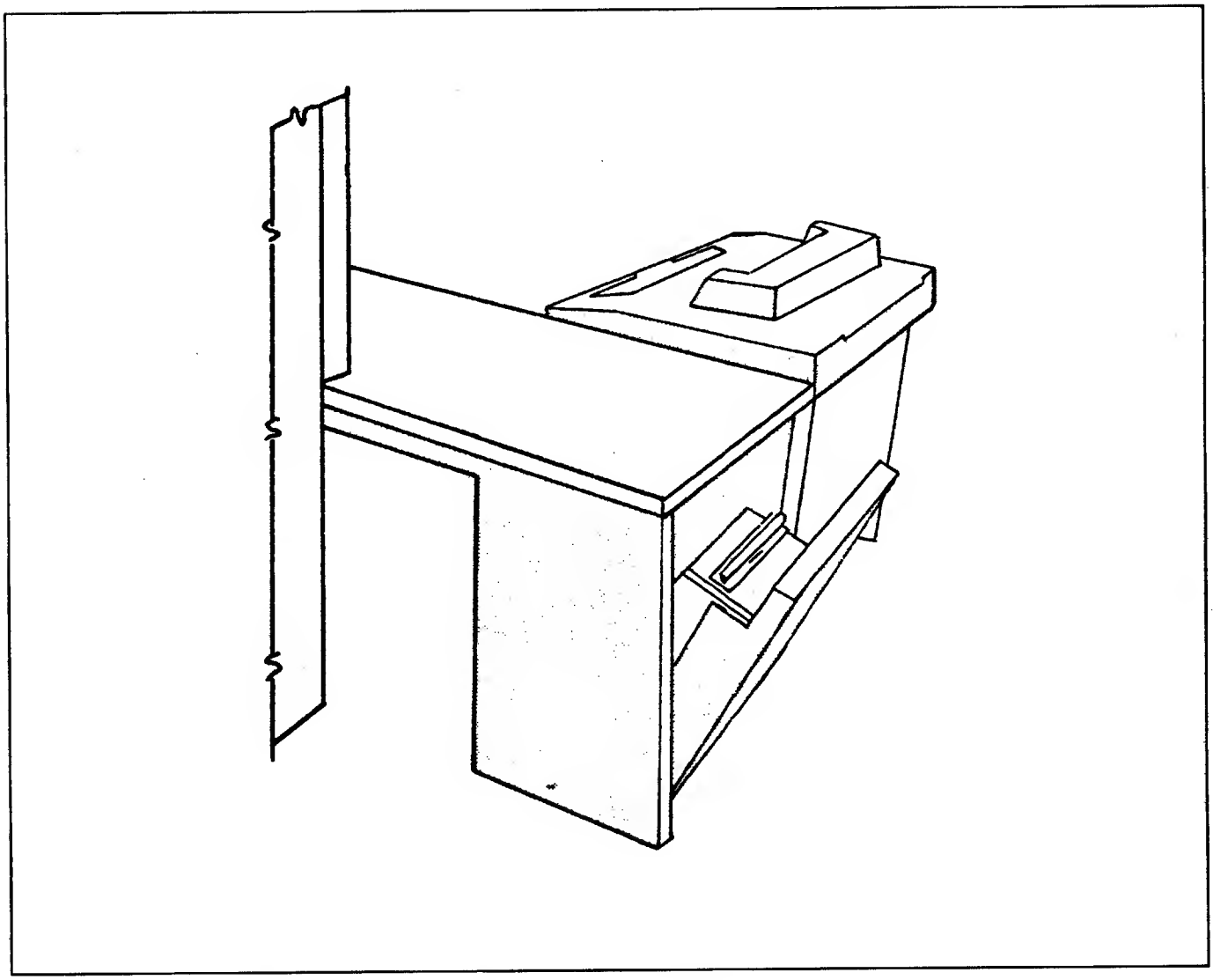

Figure 2-1. Console File

Instructions for using the console file are included in the OMEGA Operating Guide (publication number 22291360).

Initial Microprogram Loading (IMPL)

An IMPL occurs automatically when system power is applied or when the console file start key is pressed. In either case, the IMPL indicator is turned on and power is applied to the console file. When the console file attains operating speed, reading is started (CPU console switches must be set to their normal operating positions).

The microprogram is loaded from the console file into control storage. When loading is complete, console-file power is turned off, and a system reset routine is executed.

After the system reset routine is executed the CPU enters the manual state until some external action is taken (such as IPL).

CONSOLE PRINTER-KEYBOARD

The console printer-keyboard (PR-KB) is an input/output device that provides manual entry into storage, alter/display functions, and printing of program-generated messages. The device consists of a printer and a keyboard, which are linked to attachment circuitry in the CPU. The console printer-keyboard is shown in figure 2-2.

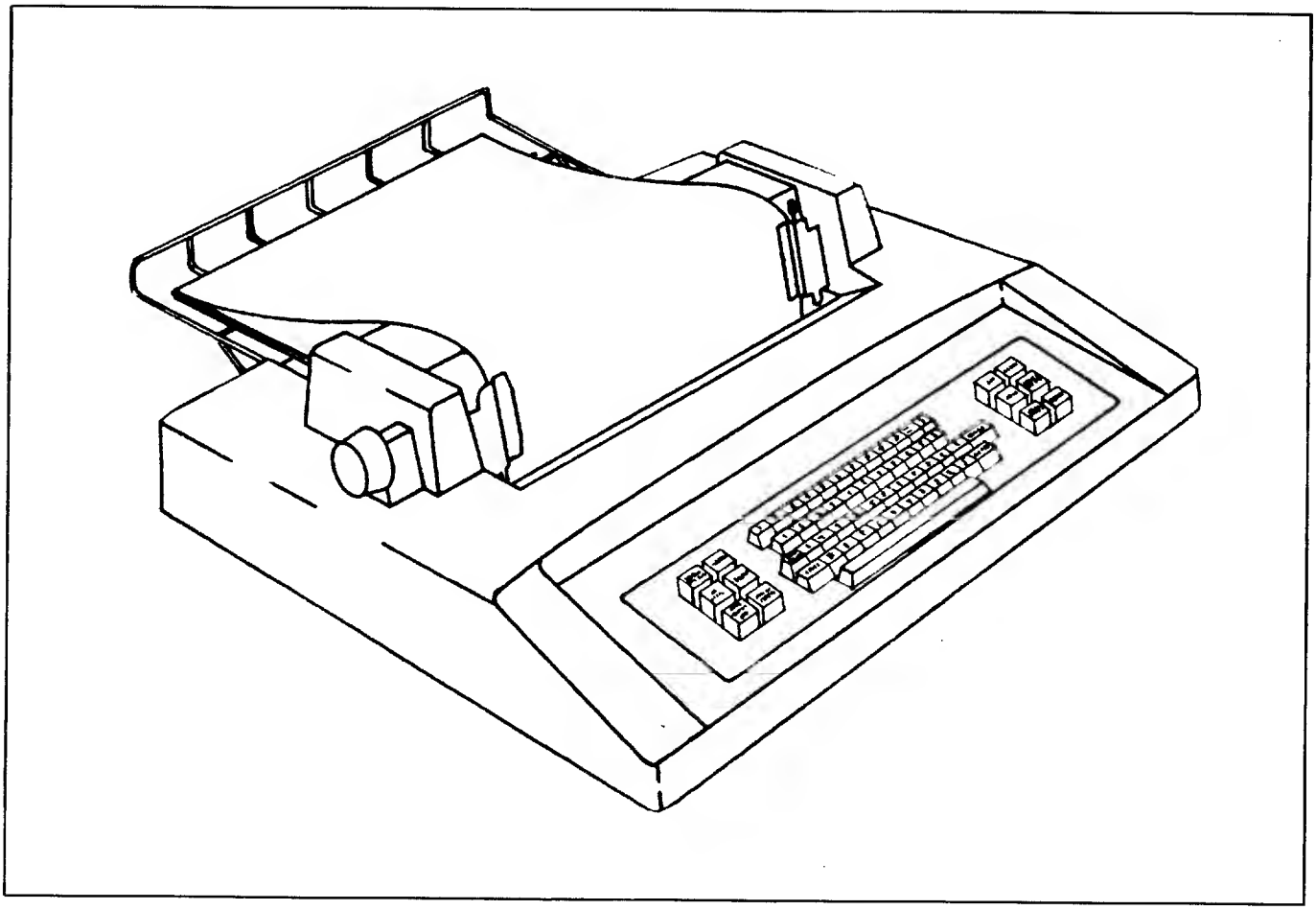

Figure 2-2. Console Printer-Keyboard

The unit prints serially (one character at a time) at a rated speed of about 60 characters per second.

Printer Functions

The printer has fixed margins and, in addition to printing, performs the following functions:

- Space

  Advance the print element one space to the right.

- New Line

  Provide a powered return of the print element to the left margin accompanied by a vertical line-feed operation.

Forms Carriage

The printer uses a pin-feed platen for positive feeding of continuous forms having a hole-to-hole width of adjustable 13-1/8 inches (333.4 millimeters).

Vertical line spacing is six lines per inch. The horizontal print line is 12.5 inches (317.5 millimeters) long, or a maximum of 125 character spaces (ten character spaces to the inch).

Keyboard

The keyboard contains 44 character keys in addition to shift, shift lock, and return keys. The tab and backspace keys are not used.

Each of the graphic character keys represents two characters. The character to be entered is selected by using the shift key. Figure 2-3 shows the arrangement of the character and function keys as well as the control switches and indicator lights.

Detailed information on the function of each of the nongraphic (control) keys is found in the OMEGA Operating Guide (publication number 22291360).

EBCDIC Graphic Code Set

Representations of the EBCDIC graphic set and associated code bits are shown in figure 2-4.

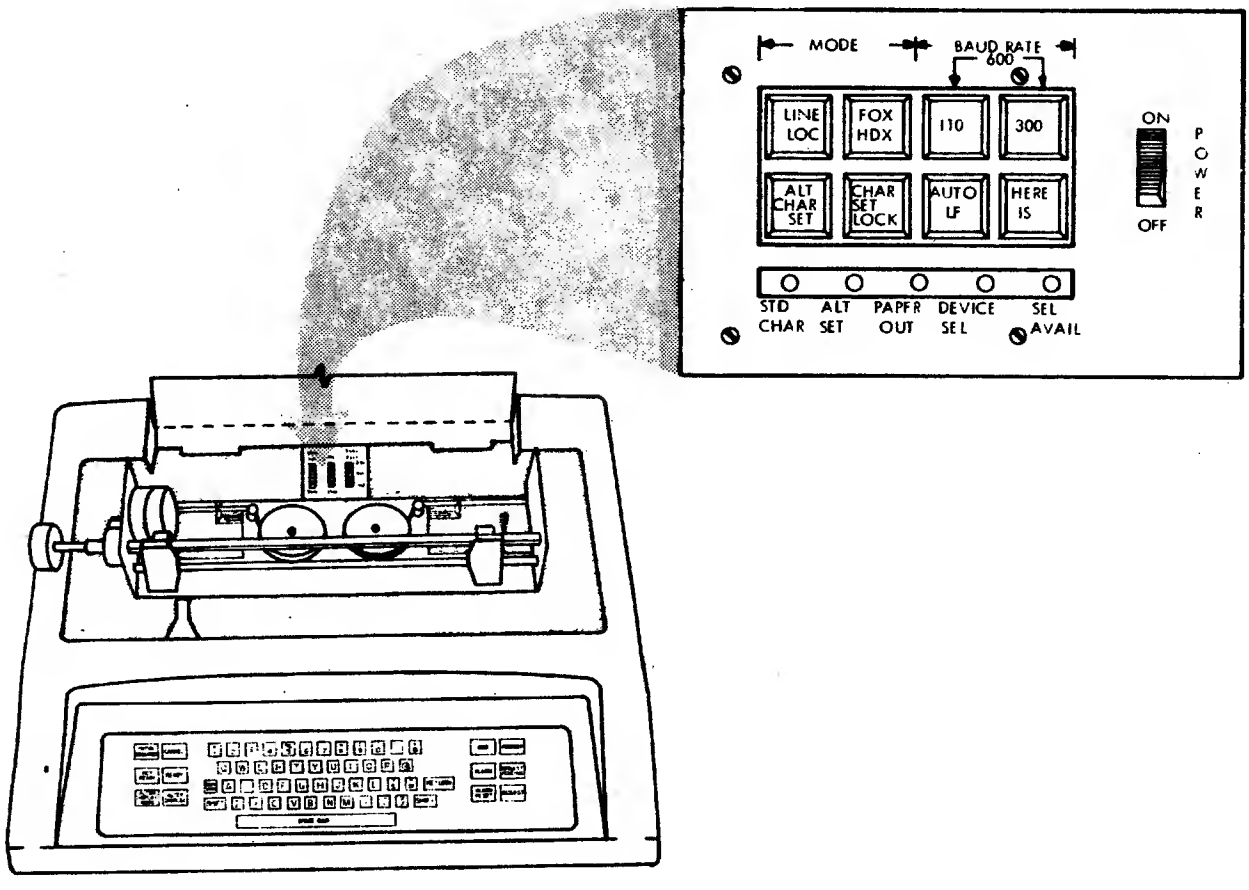

Figure 2-3. Printer-Keyboard Keys, Lights, and Switch Arrangement

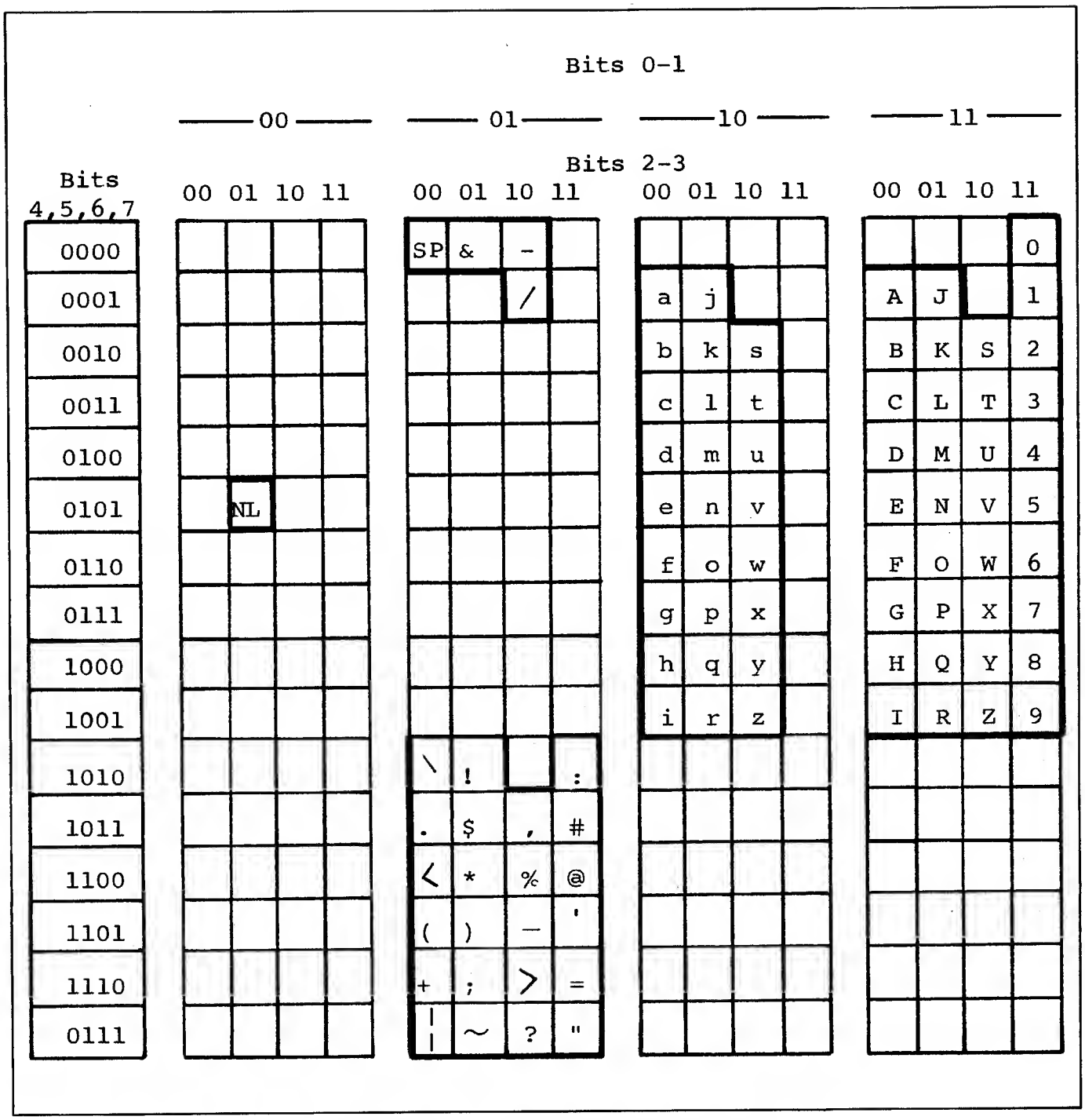

Figure 2-4. EBCDIC Graphic Code Set

Programming Information for Printer Keyboard

Printer-keyboard operations are compatible with programs written for the 1052 Model 7 Printer-Keyboard and the 3210 and 3215 Printer-Keyboard.

The printer-keyboard is attached to the byte multiplexer channel and usually has a device address of 01F.

In addition to program-controlled operations, microprogram-controlled alter/display functions are provided by the PR-KB. The alter/display function may be requested by pressing the alter/display key. The primary function of this operation is to provide a means of altering or displaying main storage, general-purpose register, floating-point registers, and other facilities. These facilities are described in the section on alter display operation in the OMEGA Operating Guide (publication number 22291360).

Status or sense information is not applicable to alter/display functions. However, the alter/display function is not executed until any current program-controlled operation is completed to the point at which status for the operation is presented to the CPU.

If an alter/display operation is started, any CPU instruction execution is delayed until after the alter/display operation is completed. Therefore, initial selection status for an I/O instruction cannot be obtained while the alter/display operation is in progress. This is because the I/O instruction cannot be executed.

Operation

The facilities provided by the console I/O unit are:

- Direct data entry from the keyboard
- Printed output from the system
- A variable-volume audible alarm from the CPU
- Switches and indicators for the control of the console I/O functions

Addressing

The console I/O unit has one address. This address consists of an eight-bit byte plus parity and can be set to any one of the possible 256 addresses at installation time.

Commands

The console I/O unit performs the same command operations as the IBM 1052-7 on System/360. These commands are as follows:

Command Byte	Command Name
0000 0100	Sense
0000 0011	Control (No-op)
0000 1011	Control (Alarm)
0000 1001	Write (Automatic Carrier Return)
0000 0001	Write (Inhibit Carrier Return)
0000 1010	Read
xxxx 1000	Transfer in Channel (TIC)

Any command code issued to the console I/O unit with a bit configuration other than those listed results in unit check (status bit 6) and command reject (sense bit 0) indications.

SENSE

The sense byte is read from the control unit and is placed in the main-storage location specified by the address in the sense command. If the unit is not operational, the sense command is still executed. The intervention required bit is on. The byte count in the sense command should be 1. If the count is greater than 1, an incorrect-length (IL) indication results, provided that the SLI flag is off. Channel end and device end status bits are presented in the CSW stored by a subsequent I/O interruption (or cleared by test I/O) for the sense operation.

CONTROL (NO-OP)

No-op is an immediate command that is processed regardless of whether the console I/O unit is operational. Unit check and intervention required bits are not set on when a no-op command to a nonoperational unit is executed.

Channel end and device end status bits are set in the CSW stored for a start I/O initial selection that called for a no-op command (provided command chaining is not in progress).

ALARM (AUDIBLE)(0000 1011)

This control command is an immediate command and functions in the same manner as a no-op, except that an alarm sounds in the CPU when this control command is executed.

Under program control, the audible alarm signals the operator when the system requires manual attention. When the program issues the alarm command, the feature emits an audio tone and turns on the alarm indicator on the printer-keyboard. The tone sounds for about 1.5 seconds, but the indicator remains lighted until the operator presses the alarm reset key on the printer-keyboard. The alarm intensity is adjustable.

An alarm command is executed even if the PR-KB is in the not-ready state.

WRITE (AUTOMATIC CARRIER RETURN)

The write command is accepted by the console I/O unit only if the following conditions are satisfied:

- The unit is ready; that is, the forms are in place and the not-ready key has not been pressed. (The intervention required light is off when the unit is operational.)
- The write command has a valid format. The byte count is not 0, the data address is valid, and so forth.
- The unit is not busy.

If the unit is not ready, condition code 1 is set and unit check status in the CSW is stored for the start I/O initiating the write command, or is stored on a subsequent I/O interruption (or test I/O) if chaining to the write command was performed.

When the print operation moves the carrier to the end of the print line, the end-of-line switch automatically initiates a new-line (carrier return and line-feed) function.

The keyboard is inoperative during a write operation. Certain control keys, however, are still active. Pressing the end key terminates the write operation in progress; an asterisk is automatically printed and an automatic NL (new line) is issued.

When the print operation is completed and the byte count reaches 0, an automatic NL function is performed. If the end-of-line switch is operated after the last character is printed, two new-line functions occur, one because of the switch and the other because of the write (ACR) command.

WRITE (INHIBIT CARRIER RETURN)

This command is performed just as the write with automatic carrier return command, except that no new-line function is performed after the byte count in the write operation reaches 0.

READ

The read command is accepted by the console I/O unit only if the unit is both ready and not busy. The proceed light turns on when the read command is accepted.

If the unit is not ready, the unit check status bit set in the CSW is stored for the start I/O initiating the read command, or is stored on a subsequent I/O interruption (or test I/O) if chaining to the read command was performed.

If the end-of-line switch is operated by the carrier after a character is printed, a new-line function occurs but the new-line character is not sent to main storage. The proceed light is off for the duration of the new-line operation.

If the end key is pressed, the read operation is ended. If the count is not 0 and the SLI flag is off, IL is indicated in the CSW stored for the operation. The end character bit pattern is not sent to main storage and nothing is printed as a result of an end key operation.

If the cancel key is pressed, unit exception status bit is set on. If the data byte count is not 0 and the SLI flag is off, IL is indicated in the CSW stored for the operation. A character is not sent to main storage, but an asterisk is printed and the carrier returns (NL function).

If the data count is down to 0, the operation is ended the next time any key is operated. The character is not sent to main storage and nothing is printed. If any key other than the end or cancel key is operated, IL is indicated in the CSW stored when the SLI flag is off.

At the end of each read operation (count equals 0, or manual end), the printer-ready condition is tested. If the printer is not ready, any chaining called for is not allowed. Unit check, channel end, device end, and intervention required bits are set on as ending status in the console I/O unit status and sense bytes.

TRANSFER IN CHANNEL

The transfer in channel (TIC) command operation is as specified in IBM System/360 Principles of Operation, GA22-6821.

Sense Byte

The sense byte information is sent to the channel in response to a sense command. The sense byte format is:

Bit	Definition
0	Command Reject
1	Intervention Required
2	Bus-Out Check
3	Equipment Check
4-7	Not Used

Unit check status bit is set on whenever one or more of the sense bits are set on. The sense bits are as follows:

- Command reject (sense bit 0)

  This bit is set on if a command not defined for the console I/O unit is issued.

- Intervention required (sense bit 1)

  This bit is set on when a read or write command is issued and the unit is in the not-ready state. The not-ready condition is caused by running out of paper or pressing the NOT READY control.

- Bus-out check (sense bit 2)

  This bit is set on when even parity is detected on a character sent to the unit from the CPU.

- Equipment check (sense bit 3)

  This bit is set on either when even parity is found on a keyboard-generated character.

Status Byte

The status byte is sent to the channel when status information is required during an operation. Table 2-1 gives the status byte format.

Table 2-1. Status Byte Format

Bit	Definition	CSW Position
0	Attention	32
1	Not used	33
2	Not used	34
3	Busy	35
4	Channel end	36
5	Device end	37
6	Unit check	38
7	Unit exception	39

ATTENTION (STATUS BIT 0)

This bit is set when the request key is pressed if no other operation is in progress. If another operation is in progress, pressing the request key causes the attention status bit to be turned on after status for the other operation has been cleared (accepted by the CPU program). If the other operation is an alter/display operation (for which status is not presented), the attention status bit is not set until the alter/display operation is completed.

After the attention status bit is set on:

- If an I/O interruption for the console I/O unit is processed, the CSW stored contains attention (bit 32).
- If a start I/O is executed before the I/O interruption can be processed, the CSW stored for the start I/O contains attention (bit 32) plus busy (bit 35).
- If a test I/O is executed before the I/O interruption can be processed, the CSW stored for the test I/O contains attention (bit 32).
- If a halt I/O is executed before the I/O interruption can be processed, the CSW is not stored and the condition code is 0 (interruption pending).

The first three items clear the status at the console I/O unit; the last item does not clear the status.

BUSY (STATUS BIT 3)

This bit is set in the CSW (bit 35) stored as a result of execution of a start I/O only for the following conditions:

- A program operation (other than a no-op or an alarm command) has been completed to the point at which the channel end bit has been accepted by the CPU (and an I/O interruption or test I/O instruction has been processed to store the channel end bit in a CSW), but the device end bit is now outstanding. Device end bit (CSW bit 37) accompanies the busy bit in the CSW for the start I/O, and the status at the console I/O unit is cleared.

- Attention status bit (resulting from a request-key operation) is outstanding for the console I/O unit (that is, the attention status has not yet been cleared by an I/O interruption or test I/O operation). Attention bit (CSW bit 32) accompanies the busy bit in the CSW stored for the start I/O.

- A device end bit for a not-ready-to-ready sequence (the ready switch has been operated) is outstanding at the console I/O unit. Device end (CSW bit 37) accompanies the busy bit in the CSW stored for the start I/O.

- A program operation has been completed to the point at which the channel end bit has been accepted by the CPU (an I/O interruption or test I/O instruction has been processed to store the channel end bit in the CSW), but the device end bit is not yet available. The busy bit alone is presented in the CSW for the start I/O, and the console I/O unit status is not affected.

Busy bit is stored as a result of a test I/O instruction only if it is executed after the channel end bit for a command is accepted, but before the device end bit for that same command occurs.

CHANNEL END (STATUS BIT 4)

This bit is set on for the console I/O unit under any of the following conditions:

- A byte count of 0 is found in a write (automatic carrier return), write (inhibit carrier return), read, or sense command.

- A control no-op or control alarm command is accepted and executed during initial selection.

- The end key or the cancel key is pressed during a read command operation.

- The end key is pressed during a write command operation.

- A sense command specifies a byte count greater than 1 and the console I/O unit terminates the operation after one byte is transferred (normal operation).

Channel end bit alone, either held in the byte-multiplexer channel or stacked at the console I/O unit, is cleared by an I/O interruption or by test I/O and is stored in the CSW.

DEVICE END (STATUS BIT 5)

This bit is set on for the console I/O unit under any of the following conditions:

- A carrier return function ends for a read or write (automatic carrier return) operation.
- The function immediately following the 0-count condition for the write (inhibit carrier return) operation is initiated.
- The console I/O unit accepts a control no-op or control alarm command during initial selection.
- The ready key is pressed while the console I/O unit is not ready. The operation of the key must produce a ready condition to set the device end bit.
- The sense byte is presented to and is accepted by the CPU.

Device end bit generated by or stacked at the console I/O unit is cleared during initial selection for a start I/O only if channel end bit (as a result of the operation) has already been stored in the CSW by an I/O interruption or a test I/O. Busy bit accompanies the device end bit in the CSW stored for the start I/O. Test I/O clears any outstanding device end bit; halt I/O does not clear the device end bit.

UNIT CHECK (STATUS BIT 6)

This bit is set on under any of the following conditions:

- A character with even parity is sent from the keyboard to the CPU during a read command operation. Equipment check bit (sense bit 3) is also set on for this condition.
- If a parity error is detected on data during a write operation, a check condition is indicated in the same manner as for other byte multiplexer channel operations.
- The forms switch indicates that the unit is out of paper or in the not-ready condition, but then only:

  a. During a read or write (either type) command operation.

  b. At initial selection for a read or write (either type) command.

  c. During execution of a test I/O instruction to the console I/O unit. Intervention required bit (sense bit 1) is also set on for this condition.

  An invlaid command byte is sent to the console I/O unit. Command reject bit (sense bit 0) is also set on for this condition.

UNIT EXCEPTION (STATUS BIT 7)

This bit is set on if the cancel key is operated during a read command operation. The read operation is terminated (channel end status bit is set on). If the byte count is not 0 and the SLI flag is off for the read command, the incorrect-length

indication (CSW bit 41) is also given during a subsequent I/O interruption or test I/O operation.

Operator Controls

Table 2-2 lists (alphabetically) all operator controls and indicators and their implementation.

Table 2-2. Operator Controls and Indicators

Name	Implementation
Alarm	Light
Alarm Reset	Key
Alter/Display	Key
Alter/Display	Light
Cancel	Key
End	Key
Intervention Required	Light
Not Ready	Key
Proceed	Light
Ready	Key
Request	Key
Request Pending	Light

- Alarm

  The alarm light indicates that the control alarm command has been issued to the console I/O unit.

- Alarm Reset

  Pressing the alarm reset key resets the alarm condition and turns off the alarm light.

- Alter/Display (Key)

  Pressing the alter/display key causes entry into alter/display mode if the system is in manual mode and the unit is not executing a read operation and not engaged in channel initiated selection. See the section on alter/display operation.

- Alter/Display (Light)

  The alter/display light indicates that the console I/O unit can only be used for display and alter operations.

- Cancel

  The cancel key is active only during a read operation. Pressing the cancel key causes the operation to terminate with unit exception status. An asterisk is printed and an automatic NL function occurs.

- End

  The end key replaces the EOB on the IBM 1052-7. The end key is active during read, write, and carrier return operations. Pressing the end key terminates the data transfer operation. If the end key is used to halt a write operation, an asterisk is printed. The carrier is returned (NL function).

- Intervention Required

  The intervention required light indicates that the unit is in a not-ready state. The not-ready key was pressed while the unit was properly conditioned, or paper forms are not in the machine.

- Not Ready

  Pressing the not ready key causes the console I/O unit to become not ready, provided that the unit is not busy and not engaged in channel-initiated selection.

- Proceed

  The proceed light indicates that a read command is initiated and a character may be entered by the operator.

- Ready

  Pressing the ready key causes the console I/O unit to become ready, provided paper forms are present and the unit is properly conditioned.

- Request

  Pressing the request key causes an attention interruption if the unit is not busy and not engaged in channel-initiated selection. If the unit is so occupied, the key action is remembered and the interruption is generated when the conditions allow.

- Request Pending

  The request pending light indicates that a request key operation still needs to be serviced.

ALTER/DISPLAY OPERATION

The alter/display operation provides both an access to various CPU areas and the means of either altering or displaying the contents of these areas. The console printer keyboard supplies a printout record of alter/display operations undertaken.

The alter/display function is initiated as follows:

1. The operator presses the STOP or SYSTEM RESET button on the system control panel of the CPU.

2. The MANUAL indicator on the system control panel is lit indicating that the CPU has entered the manual stop state.

3. The operator presses the ALTER/DISPLAY button on the console printer keyboard.

4. The ALTER/DISPLAY MODE indicator on the console printer keyboard is lit, the MANUAL indicator goes out, and a carrier-return and line-feed operation occurs. The START and RESET buttons are disabled.

5. The PROCEED indicator on the console printer-keyboard is lit, indicating that the alter/display operation may begin.

The operator enters, at the keyboard, a one- or two-character mnemonic that specifies the type of function needed and the storage area to which access is required.

For alter or display:

First character: A (alter) or D (display)

Second character: one of the designations shown in table 2-3 for the storage area

For store status: ST (see store status in this section)

For test: T (see test mode in this section)

When the operator keys in the second character (except P or T) of the mnemonic, the machine automatically leaves a space; the operator must then enter, in hexadecimal notation (see table 2-3) the required address within the storage area specified. If the second character is P (for PSW), no address or register number is necessary, and the machine automatically takes a new line. A second character of T can only be used for store status.

If the alter function has been specified, the microprogram accepts further hexadecimal data from the keyboard and places it in the specified storage area. If display has been specified, the console printer keyboard prints out the data that is contained in the specified storage area. The microprogram accepts uppercase or lowercase characters from the keyboard, but the printer output is in uppercase characters.

If any one of the following conditions occurs, the character that has been keyed in is not printed:

- The first character entered for the mnemonic is other than A, D, S, or T.
- The second character entered is not as given in table 2-3.

- Any data character is not a valid hexadecimal code.

No action is taken for these conditions, but the adapter waits for the correct key entry to be made, and normal operation is then continued.

Storage Address

The address or register number of the location specified for the alter/display function must be of the correct length for the mnemonic and must consist of valid hexadecimal characters. If not, or if the storage address is invalid (that is, outside the range of storage) or if a floating-point register number is not 0, 2, 4, or 6, the machine prints the message. It then takes a new line so that the keyboard is set up for a new operation.

Storage protection does not apply to alter/display operations because a protection key of 0 is used. The address for the storage-protection key function does not have to be on any special boundary.

Table 2-3. Alter/Display Function Mnemonics

Mnemonic Characters		Definition	Associated Address Length (Hex Characters)
First	Second		
A		Alter	
D		Display	
	M	Main Storage	6
	G	General Register	1
	F	Floating-point register	1
	P	PSW	0
	C	Control Register	1
	K	Storage Protection Key	6
	V	Virtual Storage	6
S	T	Store Status	0

Store Status

Store status, initiated when the operator enters the characters ST at the keyboard, places the PSW and the program-addressable registers in permanently assigned main storage locations, as shown in table 2-4. The contents of the PSW and registers remain unchanged.

Table 2-4. Permanently Assigned Main Storage Locations

	Main Storage Address (Decimal)	Length of Field (Bytes)
PSW	256	8
Floating-point registers (0-6)	352	32
General Registers (0-15)	384	64
Control Registers (0-15)	448	64

Test Mode

After entering test mode, the console I/O unit acts as a typewriter; all characters are printed as input. No changes are made to any system facilities. The test feature permits any character, space, or NL key to be tested for input, output, and mechanical action.

Data Format

All alter/display functions are formatted in words of eight digits and the words are separated by double spaces, with up to eight words per line. The spacing and carrier controls are automatic.

If the storage address is not on a fullword boundary, spaces are provided automatically in the first words so that subsequent groups of eight digits represent fullwords on boundaries. The operation continues indefinitely, unless terminated. New lines are taken as necessary until the end of the storage area is reached. In the case of a main storage operation, the end of the storage area is the last byte in addressable memory; in the case of a virtual storage operation, the end of the storage area is the last byte in the page containing the initial address. A new line is then taken, and the message is printed if an attempt is made to alter or display an invalid address.

The format of the PSW consists of one line of two words. The register operations for floating-point registers are formatted in one line and for general registers and control registers in two lines, with eight words per line. Each operation starts from the register number that is specified and continues, returning to 0 as necessary, until all registers are altered or displayed.

Storage keys are also formatted as words of eight digits. Each word consists of 4 two-digit keys for successive 2,048-byte blocks of storage. When the end of storage is reached, a new line is taken and the message is printed if an attempt is made to alter or display the invalid address.

Ending of Operation

Any one of the following conditions ends an alter/display operation:

- An invalid address was specified initially
- The end of the storage area is reached or all registers have been dealt with
- The ALTER/DISPLAY button is pressed again during an alter/display operation
- The END button is pressed during the operation

For the first two items, the machine prints an error message and takes a new line, the carrier returns, and the console printer-keyboard is set up for a new operation. Similar results apply for the third item, except that no error message occurs. For the last item, the console printer-keyboard takes a new line, the carrier returns, the ALTER/DISPLAY MODE indicator goes out, and the CPU returns to the stopped state.

Alter/Display Sense and Status Information

Sense and status information is not applicable to alter/display functions. However, the alter/display operation cannot be initiated until any current program-controlled operation is completed to the point at which status for that operation is presented to the CPU.

Alter/Display Manual Controls and Indicators

The alter/display manual controls and indicators are as follows:

- Alter/Display Key/Light

  The alter/display key is interlocked to be operative only when the machine is in the stopped state (manual light on). Pressing the alter/display key turns on the alter/display light. Pressing the alter/display key while the alter/display light is on terminates the alter/display operation, causes an NL function, and leaves the unit in alter/display mode.

  The alter/display mode light turns on to show that the console I/O unit is capable of performing an alter/display operation. This light turns on when the alter/display key is pressed (and acknowledged); this light turns off when alter/display is no longer in effect after the end key is pressed.

- Cancel Key

  Cancel is not a valid alter/display operation. Pressing the cancel key is ignored in alter/display mode.

- End Key

  Pressing the end key initiates the termination of alter/display mode. The alter/display mode light turns off and the console I/O unit is inoperative. The CPU returns to the stopped state (manual light on).

- Proceed Light

  The proceed light is on when the keyboard is operative and capable of receiving keyed data from the operator. While the alter/display functions are performing automatic formatting operations on the unit, the keyboard becomes inoperative and the proceed light turns off.

Section 3. Features

Refer to the IBM System/370 Principles of Operation, GA22-7000, or other sections of this manual, for system features not described here.

BYTE-ORIENTED OPERAND FEATURE

The byte-oriented operand feature allows the main storage operands of nonprivileged instructions to appear on any byte boundary without causing a specification exception and a program interruption. When operands for word operations are not on word boundaries, or operands for halfword operations are not on halfword boundaries, performance degradation can be expected. This feature does not apply to the alignment of instructions or channel command words (CCW's).

EXTENDED EXTERNAL MASKING

The extended external masking feature provides for selective masking of interruptions that are caused by timer, interrupt key, and external signals 2 through 7.

Masking is controlled by three subclass mask bits in control register 0, defined as follows:

- Internal timer mask (T)

  Bit 24 of control register 0 controls whether the CPU is enabled for a timer interruption. An external interruption caused by the timer value becoming negative can occur only when both the external mask bit in the PSW and the timer mask bit in control register 0 are ones. (The T-bit is unaffected by system reset.)

- Key mask (K)

  Bit 25 of control register 0 controls whether the CPU is enabled for interruptions due to a signal from the interrupt key. An interruption from this source can occur only when both the external mask bit in the PSW and the key mask bit in control register 0 are ones. (The K-bit is unaffected by system reset.)

FLOATING-POINT FEATURE

Both the IBM System/360 floating-point feature instructions and the extended-precision instructions are included in the OMEGA floating-point feature. The extended-precision instructions can handle extended-precision (28-hexadecimal-digit) floating-point operands. Extended-precision operands can also be rounded to long-precision format and long-precision operands can be rounded to short-precision format. For further information, see the IBM System/370 Principles of Operation, GA22-7000.

STORAGE PROTECTION (STORE AND FETCH)

Storage protection (during both storage and retrieval of data and instruction) is standard on OMEGA. The storage-protection feature makes it possible to protect the contents of storage from unauthorized access or inadvertent destruction.

OS/DOS COMPATIBILITY

The OS/DOS compatibility feature allows execution of DOS programs by emulation while the OS supervisor is controlling the system operation. Refer to the IBM System/360 OS Program Planning Guide for the DOS Emulator on the System/370, GC24-5076.

The emulated environment must be a single continuous block in main storage.

Special instructions are provided to assist the emulation process. The basic operation of the instructions is performed through a microprogram. These instructions are unique to the OS/DOS compatibility feature and are intended and supported only for use by the integrated emulator program.

INTERVAL TIMER

The interval timer provides program interruptions on a program controlled time basis. Uses of the interval timer include:

- Job accounting
- Monitoring for perpetual program loops
- Time stamping
- Polling at timed intervals

The storage word at main-storage location 50 (hexadecimal) is reserved for the interval timer feature. Any value stored at this location is automatically reduced by decrementing bit 23 every 3.3 milliseconds, provided the interval-timer switch is in the NORMAL position.

The program in process can be automatically interrupted by an external interruption (if PSW system-mask bit 7 and bit 24 in control register 0 are ones) when the interval-timer word goes from a positive value to a negative value. The interruption is identified by setting the appropriate bit on in the interruption code.

The high-order 24 bits of the interval-timer word are used to provide a full cycle of about 15.5 hours.

Interval-Timer Switch

When the interval-timer switch is set to the NORMAL position, the value stored in the interval-timer word is automatically decremented immediately after being restored.

When the switch is in the DISABLE position, no decrementing of the interval-timer word takes place. The four bytes may be used for normal program applications. Displaying main storage location 50 (hexadecimal) under this condition displays the last information stored. This information could be either the interval time setting or other program information.

TIME-OF-DAY CLOCK FEATURE

The time-of-day clock provides an accurate measure of time, independent of system events or activities and makes measurement available for programming applications. When system power is turned off, the clock value is lost. Once the time-of-day clock has been made operational through the set clock instruction and the TOD CLK switch, it maintains a constant rate of increase. The full cycle of the clock is about 143 years. This timing operation is not affected by:

- Any normal activity or event in the system
- Wait state
- Stopped state
- Instruction-step mode
- System reset
- Initial program load procedure

The time-of-day clock is an internal doubleword binary counter. Time is measured by incrementing bit position 51 by one every microsecond, following the rules for fixed-point arithmetic.

When the clock is being set, bits 52 through 63 of the designated doubleword value are ignored and are not used as part of the clock value. When the clock value is stored, bits 52 through 63 of the clock value are automatically zeroed.

Time-of-Day Clock Instructions

The clock value can be accessed by the store clock instruction. It causes the current clock value to be stored in a main storage location specified by the instruction.

The clock can be set to a specific value by the privileged set-clock instruction. This instruction causes the current clock value to be replaced by the value specified in the instruction. The set-clock instruction changes the clock value only when the TOD CLK switch is in the ENABLE SET position.

DOUBLE WORD BUFFER

The channel double-word-buffer feature increases efficiency of the system because it permits the assembly of up to 16 bytes of data before requiring a data transfer. Thus the channel speeds and the CPU throughput are greatly improved.

NOTE

Data transfers on the interface are still one byte at a time, but the number of data accesses to main storage are fewer.

The double-word-buffer feature is effective on all attached block-multiplexer channels.

VIRTUAL MACHINE ASSIST FEATURE

The virtual machine assist (VMA) feature provides a reduction in real supervisor state time and an increase in batch throughput when operating under VM/370 supervisors. Selected privileged operations and interruptions are emulated.

Because all supervisors operating under VM/370 execute in problem program mode, privileged operations are intercepted and simulated by VM/370 with macro routines. The virtual machine assist feature intercepts certain privileged operations and interrupts before they are passed to VM/370 and emulates the routines.

The following privileged instructions and interrupts are emulated by VMA:

IPK	LPSW	SSM
SPKA	ISK	SVC interrupt
STOSM	SSK	Page invalid interrupt
LRA	STCTL	
STNSM		

EXTENDED CONTROL FEATURE

The extended control (EC) feature provides a means of initiating and reporting a number of extended functions. However, the system can still operate in basic control (BC) mode to accommodate programs written for IBM System/360.

An EC PSW format, control registers, and an extension to the permanently assigned storage area comprise the EC mode. Bit 12 of both the BC mode and the EC mode formats of the PSW have a common notation for identification. When bit 12 is set to 0, the PSW is identified as BC mode. When bit 12 is set to 1, the PSW is identified as EC mode. The change from one mode to another can be made with any PSW interchange. For example, an I/O operation can be started in one mode and continued to an ending in another mode.

Mask bits for extended features replace the system mask of the BC PSW. The system mask is moved to the control registers. The condition code (CC) and the program mask (PM) fields are moved to the interruption code area of the BC PSW. The instruction length code (ILC) and the interruption codes are moved to an area of permanently assigned storage.

EC mode provides mask bits for the following functions:

- Program-event recording (bit 1)

  This feature allows the programmer to debug his program through identification of instructions that could cause trouble in operation. These include branch instructions, fetch instructions, storage alteration, and general register alterations. The recognition of one of these conditions causes a program interruption with the instruction address and code posted in a main storage location.

- Dynamic address translation (bit 5)

  This feature allows the conversion of programs expressed in virtual addresses to real addresses in main storage. The translation does not occur for I/O addresses or permanently assigned addresses used by the CPU. The I/O counterpart for this feature is the channel-indirect data addressing feature that is not masked and is allowed in either BC or EC mode.

- Input/output mask (bit 6)

  The I/O masks that allow interruptions for I/O channels selectively are located in control register 2. The mask bit in the EC PSW represents a master mask.

- External mask (bit 7)

  The external masks that allow interruptions for external devices selectively are located in control register 0. The mask bit in the EC PSW represents a master mask.

Figure 3-1 shows the related mask bits, features, and control registers associated with extended control mode. Further details about these features can be found in other sections of this manual or in the IBM System/370 Principles of Operation, GA22-7000.

The extended control feature uses two instructions that can change the mask bits in the EC PSW. The store-then-AND-system-mask instruction permits the program to turn off selected bits in the system mask while retaining the original contents for later restoration. For example, in EC mode it may be necessary for a program which is not aware of the present status to disable program-event recording for instructions.

The store-then-OR-system-mask instruction permits the program to turn on selected bits in the system mask while retaining the original contents for later restoration. For example, in EC mode the program may want to enable priority interrupts and yet may not know the current status of the I/O and external mask bits.

When the set-system-mask-suppression facility is employed, the execution of the set-system-mask instruction is subject to the set-system-mask-suppression bit (bit 1 of control register 0). When this bit is set to zero, the instruction is executed normally. When this bit is set to one, the operation is suppressed, and a special-operation exception is recognized.

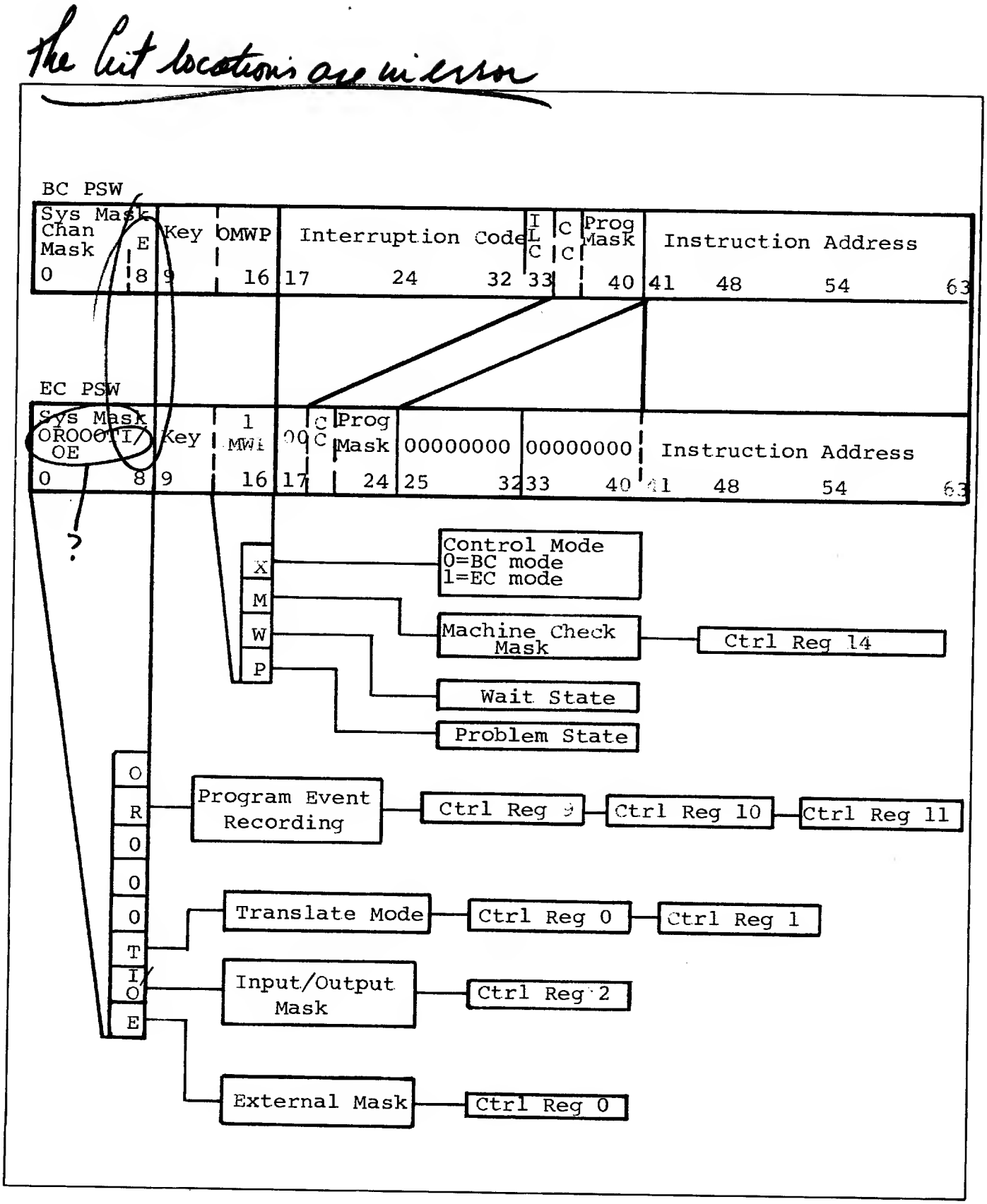

Figure 3-1. Extended Control PSW

STORE STATUS

The store status feature includes an operator-initiated function called store status, and a modification to some system reset conditions. The store status function places the contents of the programmable registers in fixed locations within the first 512 bytes of main storage. The programmable registers are stored in absolute locations as shown in table 3-1.

Table 3-1. Absolute Locations of Programmable Registers

Description	Length in Bytes	Absolute Address of First Byte Stored	
		Decimal	Hexadecimal
CPU Timer	8	216	D8
Clock comparator	8	224	E0
Current PSW	8	256	100
Floating-point registers 0-6	32	352	160
General registers 0-15	64	384	180
Control registers 0-15	64	448	1C0

The store-status function is performed by the alter/display facilities of the console printer-keyboard. Detailed instructions to perform this function are found in the OMEGA Operating Guide (publication number 22291360).

Detailed effects of the various reset functions are shown in table 3-2.

Table 3-2. Effects of Reset Functions

Area Affected	Power On	Reset Functions		
		Enable System Clear With System Reset or Load	Initial Program Load	System Reset
Control storage	M	U	U	U
TOD clock	C	U	U	U
Processor storage	C	C	U	U
Keys in storage	C	C	U	U
General registers	C	C	U	U
Floating-point registers	C	C	U	U
Control registers	I	I	I	U
Current PSW	C	C	C	U
CPU timer	C	C	C	U

Table 3-2. Effects of Reset Functions (cont)

Area Affected	Power On	Reset Functions		
		Enable System Clear With System Reset or Load	Initial Program Load	System Reset
Clock comparator	C	C	C	U
CPU state	S	S	L	S
Attached channels	R	R	R	R

NOTE

C - Contents are set to zeros with valid parity.

I - Contents are set to initial state.

L - The initial program load function is performed.

R - The channel is reset, the channel signals system reset on the I/O interface by dropping operational-out.

S - Execution of the current CPU operation, if any, is terminated pending interruptions and machine check conditions are cleared. The CPU enters the stopped state.

U - Contents including parity are unchanged.

V - Contents are unchanged except for parity, which may be changed to validate parity.

M - The initial microprogram load is executed.

PROGRAM EVENT RECORDING

The purpose of the program-event-recording (PER) feature is to assist in debugging programs. It permits the program to be alerted to:

- Successful execution of a branch instruction
- Alterations of the contents of designated general registers
- Fetching of an instruction from designated processor storage locations
- Alterations of the contents of designated processor storage locations

The program has control over the conditions that are considered events for recording purposes and can specify selectively one or more events to be monitored. Information concerning a program event is provided to the program by a program interruption, with the cause of the interruption being identified in the interruption code.

Information for controlling program-event recording resides in control registers 9, 10, and 11. Control register 9 specifies which events are to be monitored. Control register 10 designates the beginning of the monitored processor storage area. Control register 11 designates the end of the monitored processor storage area.

Program-event recording is available only in EC mode and is under the control of PSW bit 1, the PER mask. When the mask is 0, no program event can cause an interruption. When the mask is 1, interruptions are permitted subject to the PER control bits in control register 9. In BC mode, the PER mask has, in effect, a value of zero and program-event recording is disabled.

When a designated program event occurs, with the CPU enabled for program-event recording, a program interrupt occurs. The cause of the interruption is identified by setting bit 8 of the interruption code to 1, and by the information placed in locations 150 to 155 (decimal) of processor storage.

This feature should be used only for program debugging purposes because PER causes significant internal performance degradation.

DYNAMIC ADDRESS TRANSLATION

The dynamic-address-translation (DAT) feature provides for more efficient storage management. This feature allows a program to be written starting at a virtual address of zero and containing up to 16,777,215 bytes. The DAT feature also helps to solve storage fragmentation problems because adjacent storage location blocks are no longer necessary.

The 24-bit virtual (or logical) address consists of three parts: segment, page, and offset. The segment may contain 1,048,576 bytes, or 65,536 bytes depending on control register settings. The page may contain 4,096 bytes, or 2,048 bytes depending on control register setting. The offset denotes a particular byte within the page.

Control register 0 specifies page size and segment size. Control register 1 designates the origin and length of the segment table.

The segment table defines the origin and length of the page table and denotes the availability of the page table.

The page table contains the high-order bits of the real address of the page, and denotes the availability of the page.

The control register, segment table, and page table are maintained by the control program.

The conversion of a virtual address to a real address is done by a translation process. In OMEGA, this translation process is performed by microcode with the aid of translation logic. The results of the translation (as many as 64 virtual addresses) are stored in a set associative memory called the translation lookaside buffer (TLB). There is no performance loss due to the translation process as long as one of the pages contained in the TLB is accessed by the program.

The dynamic-address-translation feature uses the following instructions:

- Load real address
- Reset reference bit
- Purge TLB

These instructions are explained in detail in IBM/370 Principles of Operation, GA22-7000.

CHANNEL INDIRECT DATA ADDRESS

The channel-indirect-data-addressing (CIDA) feature provides the means of extending the address adjustment of the dynamic-address-translation feature to the I/O channels. A contiguous set of virtual addresses can be mapped into a noncontiguous set of pages in real storage. Because only a single data address need be in effect at a time for a channel, it is not necessary for the DAT hardware to handle the adjustment with each access. The adjustment factor is applied by the program and the real address is stored for the CIDA controls. These adjusted addresses are stored as an indirect-data-address list (IDAL) for each CCW. Each word of the list is referred to as an indirect-data-address list word (IDALW).

The operation of the CIDA feature is selective and can be used in either BC or EC mode. An IDA flag in the flag byte of the channel CCW functions as the indirect addressing switch. When the IDA flag equals 1, the normal data address of the CCW is the real address of an IDAL in main storage. This list contains one or more addresses of main storage on page boundaries that can be used in the operation.

For the byte-multiplexer channel the CIDA feature requires a fourth word in each assigned UCW. This word holds the IDAL address for the assigned device.

CLOCK COMPARATOR AND CPU TIMER

The clock comparator and CPU timer are standard features available on OMEGA.

The clock comparator provides for an interrupt when the time-of-day clock reaches a value specified by the programmer. The interrupt is allowed by setting bit 20 in control register 0, and the external mask bit in the PSW.

The CPU timer provides a high resolution (1 microsecond) timer which causes an interrupt whenever its value is zero or negative. The timer value is set by the programmer using the set CPU timer instruction. The interrupt is allowed by setting bit 21 in control register 0, and the external mask bit in the PSW.

Instructions provided with these features are:

- Set clock comparator
- Store clock comparator
- Set CPU timer
- Store CPU timer

Further details of these instuctions are found in the IBM System/370 Principles of Operation, GA22-7000.

CONDITIONAL SWAPPING FEATURE

Instructions provided with this feature are:

- Compare and swap
- Compare double and swap

ADVANCED CONTROL PROGRAM SUPPORT FEATURE

This feature provides these five instructions:

- Compare and swap
- Compare double and swap
- Clear I/O
- Insert PSW key
- Set PSW key from address

This feature includes the two instructions for the conditional swapping feature which makes the advanced control program support feature and the conditional swapping feature mutually exclusive.

When operating with the recommended IBM operating system programs, the system requires disk file storage for handling its programming sequences. Because of the data-handling speed of the system, the disk files should have the capability of the IBM 3330/3340 Series Direct Access Storage Facility (DASF).

SECTION 4

INPUT/OUTPUT CHANNEL CHARACTERISTICS

Section 4. Input/Output Channel Characteristics

I/O channels for OMEGA are, with a few variations, identical to those of IBM System/360 and System/370 models. For a description of some channel operations, refer to the OMEGA Hardware Maintenance Manual, Volume 1 (publication number 22291361) or the IBM System/370 Principles of Operation, GA22-7000. For details of the standard channel interface, refer to the IBM System/360 and System/370 I/O Interface-Channel to Control Unit Original Equipment Manufacturer's Information, GA22-6974.

For information about I/O devices attaching to the OMEGA interface, refer to IBM System/370 I/O Configurator, GA22-7002.

This section covers the basic characteristics and defines the limitations and additional capabilities of the I/O channels. The additional capabilities include new and redefined instructions, additional interface line, the block-multiplexer channel, and other extensions to IBM System/360 provided by IBM System/370.

This system offers the following channel configurations:

- A single byte-multiplexer channel
- Block-multiplexer channels 1 and 2
- Block-multiplexer channels 3 and 4

The byte-multiplexer channel can operate in either byte or burst mode. The mode is determined by the characteristics of the device operating on the channel. When a device on the byte-multiplexer channel forces burst mode, no other device can operate with the byte-multiplexer channel until the burst mode operation is completed.

In the byte mode, the single data path of the byte-multiplexer channel can be shared by a number of low-speed I/O devices operating simultaneously. The channel multiplexes data to or from these devices (one device at a time) in groups of bytes as required by the I/O device being serviced.

Block-multiplexer channels are designed to be used primarily for devices with higher data rates. Operations between a block-multiplexer channel and an operating I/O unit can be overlapped with CPU processing cycles. Block-multiplexer channel accesses to main storage during a data transfer cycle are on a double word basis due to the double word buffer feature.

The block-multiplexer channel is optimized for relatively high-speed burst operation and can multiplex complete blocks of data. It is particularly suited to buffered or cyclic devices with high data rates (such as disk storage devices). The multiplexing facility of the block-multiplexer channel allows the interleaved execution of several channel programs by the same channel.

The byte- and block-multiplexer channels operate from the same I/O instruction and command formats used on System/370 models.

STANDARD I/O INTERFACE

The standard System/360 and System/370 I/O interface is used to connect the CPU channel to I/O devices or control units. In addition to the standard System/360 I/O interface, extensions to the I/O interface operation are provided.

High-Speed Transfer

This extension to the I/O interface enables data transfer to take place (on block-multiplexer channels) faster than the data rates that would be obtained with service-in and service-out alone. It may also be used by some control units to permit the placement of a control unit at a greater distance from the channel than would otherwise be possible. This extension includes two additional tag lines, data-in and data-out.

Data-in may be alternated with service-in tag line to enable transfer of data at a higher rate than is possible if service-in alone is used. In this case, data-out is alternated with service-out as the response to data-in. Data-out is the response to data-in as service-out is the response to service-in.

I/O Error Alert

An additional tag line, disconnect-in, provides (on block- and byte-multiplexer channels) control units with the ability to alert the system of a malfunction that prevents the control unit from signaling correctly over the I/O interface.

Disconnect-in can be activated by a control unit only when it is connected to the channel (has operational-in up). The channel performs a selective reset in response to disconnect-in and indicates to the operating system the occurrence of disconnect-in by causing an I/O interruption.

Command Retry

Command retry is a combined channel-control unit procedure that can cause a command to be retried without requiring an I/O interruption.

It is a function of the control unit to determine whether the last command can be retried, based on factors such as whether operator intervention or program reorientation is required before retry.

Command retry applies only to block-multiplexer channels, and requires an additional line in the interface called mark 0-in.

INPUT/OUTPUT INTERRUPTIONS

The input/output interruption definition is extended by the addition of a new interruption condition.

Channel-Available Interruption Condition

A channel-available interruption condition is generated by a channel to signify that a previously indicated channel-busy condition no longer exists. Its purpose is to inform the program that the SIO instruction that received a channel-busy indication (condition code 2) can now be expected to be successful.

BYTE-MULTIPLEXER CHANNEL

The byte-multiplexer channel maximum byte-mode data rate is 50,000 bytes per second. The maximum burst-mode data rate is 180,000 bytes per second. Any block-multiplexer channel activity reduces the data rate for the byte-multiplexer channel.

The byte-multiplexer channel operations with attached I/O units are implemented under microprogram control. A particular status, data, or control communication with a device is coordinated by the standard-interface signal sequences between the device and the byte-multiplexer channel. Data transfer to or from main storage is on a byte basis only.

The byte-multiplexer microprogram controls data flow to and from the CPU, and the functions performed by specific registers that are used for byte-multiplexer channel operations only.

The byte-multiplexer channel contains a number of subchannels, each of which is capable of controlling one I/O device. Each subchannel has its functional control information stored in a four-word unit control word (UCW) that is contained in main storage.

When a byte-multiplexer-channel operation requires use of information in a UCW, that UCW (identified by the address of the I/O unit involved in the operation) is read from main storage. The operation specified by the UCW is then performed under microprogram control. The UCW is used, updated, and returned to main storage when the operation is completed. Hence the UCW carries a dynamic record of the operation for the I/O device assigned.

There is one assigned byte-multiplexer channel area in local storage for use in processing a single UCW. Therefore, when the UCW is being set up in that area during execution of an I/O instruction (or I/O interruption operation), service requests from other units on the byte-multiplexer channel are blocked.

Byte-Multiplexer Subchannel Capacity

There are 256 UCW's available for the byte-multiplexer channel; these are provided in the basic machine.

An unshared subchannel has a UCW that is reserved for one specified device only. For example, some devices require a UCW for exclusive use; each unit attached to a 2821 Control Unit requires a single UCW for its use. If a 2821 services two 1403 Printers and a 2540 Reader-Punch, four UCW's are required (two for the printers, one for the reader, and one for the punch). Each of these units has its own unique unit address.

UCW Addressing

Before a command for operation of an I/O device can be sent to its control unit, the device must be addressed. The address is derived from the I/O instruction and consists of the two low-order bytes of the developed address. The channel address (A in figure 4-1) is in the high-order byte, and the device address (B) is in the low-order byte.

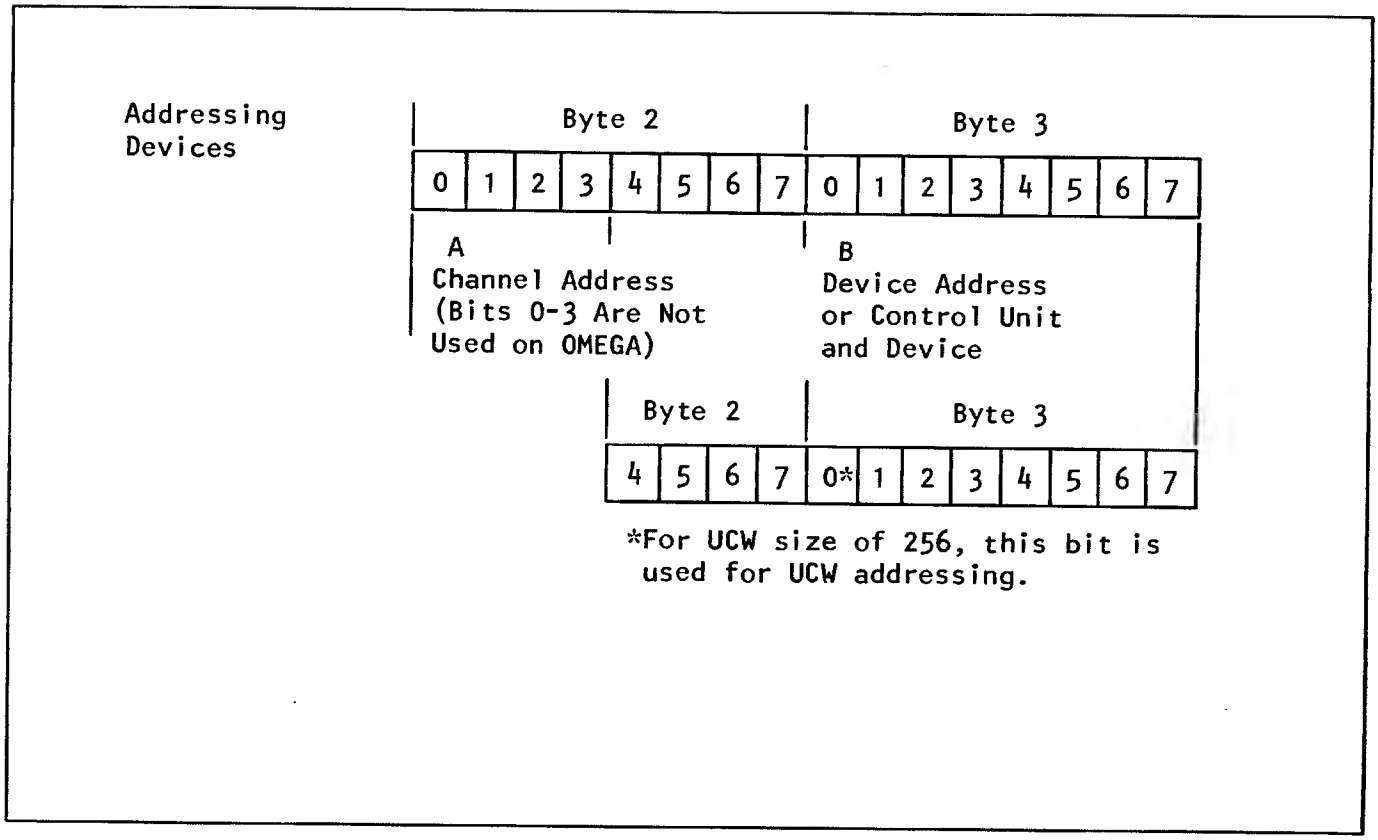

Figure 4-1. UCW Addressing

The number of subchannels used is also dependent upon the characteristics of the devices on the channel, as pointed out in the following description.

The electrical characteristics of the channel allow for up to eight I/O control-unit positions, connected serially. Positions for units on the I/O interface can be thought of in three ways, depending upon the units involved:

- A single control unit that controls one I/O unit can be connected to the channel. An example of this type of unit is the IBM 1443 Printer Model N1. One control-unit position is needed.

- A single unit that contains several control units can be connected to the channel. An example is the 2821 Control Unit, which has separate control units for each attached 1403 Printer, one for the 2540 Reader Section, and one for the 2540 Punch Section. One control unit position is needed.

- A single control unit that services the requirements of several I/O units (one at a time) can be connected to the channel. An example is a tape control unit that controls several tape drives. One control-unit position is needed.

Assume, for example, that eight 1443 Model N1 printers are attached to the byte-multiplexer channel. All eight positions are then used, and no other unit can be attached to the channel. Any eight of the subchannels could then be used for the printers, according to the device address.

BLOCK-MULTIPLEXER CHANNELS

Block-multiplexer channels are standard features on OMEGA. The block-multiplexer channels are designed primarily for use with devices that have high data rates, such as magnetic tape, drum storage, and disk-storage units. The block-multiplexer feature allows concurrent operation of many I/O devices on a channel by multiplexing blocks of data on the channel's single data path. Two to four block-multiplexer channels are available.

The data rate is maximized due to the standard double word buffer feature which is installed, however, the average data rates are dependent on the number of channels in use.

Another unique feature of the OMEGA block-multiplexer channels is the minimal interference with the CPU. After initial selection is complete, no break-in for microcode is required for data transfer. This allows processing to continue in the CPU during data transfer.

Although only one device may actually be transmitting data at any instant, multiple channel programs may be concurrently active.

Block multiplexing involves temporarily disconnecting an operation in a sequence of chained channel commands. This frees the channel during nondata transfer activity of the device and, thereby allows other devices access to the channel during this time. The block-multiplexer channels would normally attach I/O equipment that has high data rates.

The block-multiplexer channels are capable of operating in selector channel mode where they control one operation at a time. Each operation is performed in burst mode; the other devices will not be operated during this period. The channel would normally only operate in this mode if the devices on it were not capable of being multiplexed.

Block-multiplexer channel service requests are used for data transfer and skip operations but are not used for status transfer. A service-request operation is initiated by a request from the channel that required service.

Device Addressing

The channel addresses are 01 through 04. Device addressing on the block-multiplexer channel may be any of the 256 possible bit combinations of a byte.

Block-Multiplexer Channel UCW Assignments

The 256 possible device addresses on a block-multiplexer channel are divided into 16 groups of 16 device addresses. Each block-multiplexer channel has a UCW address table with a halfword entry for each device address group. The halfword entry in the table translates the actual UCW addresses from the device addresses as needed.

Each device address group is one of two types according to the UCW requirements of the devices that are to be attached. All devices in a group must have the same UCW requirements. The two types are as follows:

- Each device of the group requires an unshared UCW.
- All the devices of the group use the same shared UCW.

SECTION 5

SYSTEM CONFIGURATOR

Section 5. System Configurator

The minimum system configuration for practical applications should include a card reader (or card reader/punch); a console printer-keyboard; and either two direct access devices, or one direct access device and two magnetic tape units, or three magnetic tape units.

OMEGA STANDARD FEATURES

The following are standard features on OMEGA:

- OMEGA processing unit - 256K to 2048K bytes of main storage in 256K byte increments up to 1024K bytes and in increments of 512K bytes up to 2048K bytes
- Advanced control program support
- Audible alarm
- Block-multiplexer channels 1 and 2
- Byte-multiplexer channel
- Byte-oriented operand
- Channel indirect data address
- Channel retry information
- Conditional swapping
- Console file
- Control registers
- Dynamic address translation
- Error checking and correction (ECC)
- Extended control
- Floating-point instruction set and floating-point (includes extended precision)
- Interval timer
- Machine-check handling
- Microprogram instruction retry
- OS/DOS compatibility
- Program-event recording

- Storage protection (Store and Fetch)
- System/370 commercial instruction set
- Time-of-day clock
- Virtual machine assist
- Double word buffer
- Clock comparator and CPU timer
- Console printer keyboard
- 12K (words) of control storage

OMEGA OPTIONAL FEATURES

- Block-multiplexer channels 3 and 4 are optional on OMEGA.
- Main storage over one megabyte to two megabytes
- Addition 4K (words), total 16K words, of control storage

NOTE

The word buffer feature is installed on all block-multiplexer channels.

SECTION 6

INSTRUCTION TIMING

Section 6. Instruction Timing

INTRODUCTION

This section contains instruction timings (in microseconds) for the OMEGA CPU. Interference due to channel activity is not included in these timings.

Table 6-1. Register Operands

Operation	Operand	Inst Time	IBM Spec
Add Register	AR	.803	1.373
Add Logical Register	ALR	.752	1.373
And Register	NR	.752	1.935
Branch and Link Register	BALR	1.406	2.550
Branch and Link Reg - No Br	BALR	1.053	1.682
Branch on Count Register	BCTR	1.305	2.152
Branch on Condition Register	BCR	1.054	1.747
NOPR Register W/R2=0	NOPR	.602	1.074
NOPR Register W/R2 NE=0	NOPR	.551	1.074
Compare Register	CR	.903	1.578
Compare Logical Register	CLR	.902	1.373
Divide Register	DR	35.733	34.183
Exclusive OR Register	XR	.753	1.935
Load Register	LR	.602	.923
Load and Test Register	LTR	.753	1.373
Load Complement Register	LCR	.853	1.575
Load Negative Register	LNR	1.003	.676
Load Negative Reg - Neg 1	LNR	.802	.000
Load Positive Register	LPR	.752	1.676
Load Positive Reg - Neg 1	LPR	1.154	.000
Multiply Register	MR	12.747	9.929
OR Register	OR	.753	1.935
Subtract Register	SR	.803	1.575
Subtract Logical Register	SLR	.752	1.373
Set Program Mask	SPM	.853	1.125
Insert Storage Key	ISK	1.505	3.698
Set Storage Key	SSK	37.089	4.170

Table 6-2. Indexed Storage Operands Without Indexing

Operation	Operand	Inst Time	IBM Spec
Add - 0,8	A	1.506	2.385
Add - 7,8	A	2.710	.000
Add Halfword - 0,8	AH	1.656	2.949
Add Halfword - 7,8	AH	2.561	.000
Add Logical	AL	1.456	2.138
Add Logical	AL	2.759	.000
And - 0,8	N	1.455	2.700
And - 7,8	N	2.760	.000
Branch and Link	BAL	1.456	2.399
Branch on Count-Taken	BCT	1.456	2.242
Branch on Condition	B	1.255	1.792
Compare	C	1.606	2.441
Compare Halfword	CH	1.757	2.949
Compare Logical	CL	1.556	2.138
Convert to Binary	CVB	7.378	.000
Convert to Binary	CVB	26.805	.000
Convert to Decimal	CVD	15.808	.000
Convert to Decimal	CVD	56.961	.000
Divide	D	34.328	34.771
Exclusive OR - 0,8	X	1.455	2.700
Exclusive OR - 1,8	X	2.659	.000
Exclusive OR - 7,8	X	2.760	.000
Execute	EX	3.664	2.979
Insert Characters - 0,8	IC	1.355	1.384
Insert Characters - 7,8	IC	1.405	.000
Load - 0,8	L	1.103	1.688

Table 6-2. Indexed Storage Operands Without Indexing (cont)

Operation	Operand	Inst Time	IBM Spec
Load - 7,8	L	2.459	.000
Load Halfword - 0,8	LH	1.355	2.295
Load Halfword - 7,8	LH	2.259	.000
Load Address - 0,8	LA	.702	1.452
Load Address - 7,8	LA	.702	.000
Multiply - 0,8	M	19.041	20.077
Multiply - 7,8	M	10.141	.000
Multiply Halfword - 0,8	MH	8.933	10.508
Multiply Halfword - 7,8	MH	11.040	.000
NOP - B2=0	NOP	.903	.000
NOP	NOP	.702	.000
OR - 0,8	O	1.455	2.700
OR - 7,8	O	2.760	.000
Store - 0,8	ST	1.103	1.497
Store - 7,8	ST	5.921	.000
Store Character - 0,8	STC	1.454	1.452
Store Character - 7,8	STC	1.454	.000
Store Halfword - 0,8	STH	1.303	1.498
Store Halfword - 7,8	STH	4.114	.000
Store Halfword-	STH	2.258	.000
Subtract - 0,8	S	1.505	2.340
Subtract - 7,8	S	2.815	.000
Subtract Halfword - 0,8	SH	1.656	2.949
Subtract Halfword - 7,8	SH	2.560	.000
Subtract Logical - 0,8	SL	1.455	2.138

Table 6-2. Indexed Storage Operands Without Indexing (cont)

Operation	Operand	Inst Time	IBM Spec
Subtract Logical - 7,8	SL	2.760	.000
Load Real Address	LRA	6.171	8.696

Table 6-3. Indexed Storage Operands With Indexing

Operation	Operand	Inst Time	IBM Spec
Add - 0,8	A	1.756	2.633
Add Halfword - 0,8	AH	1.907	3.197
Add Logical - 0,8	AL	1.706	2.386
And - 0,8	N	1.706	2.948
Branch on Count-Taken	BCT	1.707	2.490
Branch on Condition	B	1.506	2.040
Compare	C	1.857	2.689
Compare Halfword	CH	2.007	3.197
Compare Logical	CL	1.807	2.386
Convert to Binary	CVB	7.629	.000
Convert to Binary	CVB	27.054	.000
Convert to Decimal	CVD	16.058	.000
Convert to Decimal	CVD	57.208	.000
Divide	D	34.575	35.019
Exclusive OR - 0,8	X	1.706	2.948
Execute	EX	3.914	3.227
Insert Characters - 0,8	IC	1.605	2.543
Load - 0,8	L	1.354	1.936
Load Halfword - 0,8	LH	1.605	2.543
Load Address - 0,8	LA	.953	1.700
Multiply - 0,8	M	19.290	20.325
Multiply Halfword - 0,8	MH	9.184	10.756
NOP	NOP	1.153	.000
NOP	NOP	.952	.000
OR - 0,8	O	1.706	2.948
Store - 0,8	ST	1.354	1.745
Store Character - 0,8	STC	1.706	1.700
Store Halfword - 0,8	STH	1.605	1.746

Table 6-3. Indexed Storage Operands With Indexing (cont)

Operation	Operand	Inst Time	IBM Spec
Store Halfword - 4,8	STH	2.509	.000
Subtract - 0,8	S	1.756	2.588
Subtract Halfword - 0,8	SH	1.907	3.197
Subtract Logical - 0,8	SL	1.706	2.386
Load Real Address	LRA	6.423	8.944

Table 6-4. Storage Operands

Operation	Operand	Inst Time	IBM Spec
Branch on Index High	BXH	2.107	.000
Branch on Index High	BXH	1.958	.000
Branch on Index Low or Equal	BXLE	2.107	.000
Branch on Index Low or Equal	BXLE	1.958	.000
	CLM	3.160	.000
	CLM	2.308	.000
	ICM	3.060	.000
	ICM	2.308	.000
	ICM	6.222	.000
Load Multiple - 1 Register	LM	2.709	.000
	LM	8.832	.000
	SLDA	4.014	.000
	SLDA	12.545	.000
	SLDL	2.659	.000
	SLDL	7.677	.000
	SLA	2.508	.000
	SLL	1.856	.000
	SLL	2.960	.000
	SRDA	4.113	.000
	SRDA	10.688	.000
	SRDA	3.160	.000
	SRDL	2.759	.000
	SRDL	7.978	.000
	SRDL	1.956	.000
	SRA	2.458	.000
	SRA	3.763	.000

Table 6-4. Storage Operands (cont)

Operation	Operand	Inst Time	IBM Spec
	SRL	2.006	.000
	SRL	2.860	.000
	STCM	4.416	.000
	STCM	2.157	.000
	STCM	7.727	.000
Store Multiple 1 Register	STM	3.563	.000
	STM	9.936	.000
	STCTL	9.484	.000
	STCTL	22.683	.000
	LCTL	29.263	.000
	LCTL	50.038	.000
Compare and Swap - CC=0	CS	3.764	.000
Compare Double and Swap - C=0	CDS	5.570	.000

Table 6-5. Storage - Immediate Operands

Operation	Operand	Inst Time	IBM Spec
And Immediate	NI	1.806	.000
Compare Logical Immediate	CLI	1.405	.000
Exclusive or Immediate	XI	1.882	.000
Move Immediate	MVI	1.454	.000
Or Immediate	OI	1.857	.000
Test Under Mask	TM	1.355	.000
Store Then And System Mask	STNSM	5.270	.000
Store Then Or System Mask	STOSM	5.370	.000

Table 6-6. Storage - Storage Operands

Operand	Inst Time	IBM Spec
NC	6.724	.000
NC	124.000	.000
CLC	4.967	.000
CLC	98.658	.000
XC	6.724	.000
XC	124.000	.000
MVC	4.516	.000
MVC	49.384	.000
MVN	6.624	.000
MVN	127.171	.000
MVO	6.423	.000
MVO	32.721	.000
MVZ	6.624	.000
MVZ	127.172	.000
OC	6.724	.000
OC	124.010	.000
PACK	6.122	.000
PACK	20.025	.000
TR	6.925	.000
TR	617.117	.000
TRT	3.864	.000
TRT	500.757	.000
UNPK	5.569	.000
UNPK	15.406	.000

Table 6-7. Decimal Operands

Operand	Inst Time	IBM Spec
AP	11.090	.000
AP	24.992	.000
CP	11.491	.000
CP	23.518	.000
DP	17.697	.000
DP	109.932	.000
MP	14.134	.000
MP	73.166	.000
SP	13.600	.000
SP	30.513	.000
ZAP	12.094	.000
ZAP	32.168	.000
SRP	10.638	.000
SRP	14.101	.000
FD	34.157	.000
FD	64.568	.000
FDMK	34.809	.000
FDMK	65.220	.000

Table 6-8. Floating Point Register - Register Operands

Operand	Inst Time	IBM Spec
ADR	3.813	.000
AER	2.609	.000
AWR	3.061	.000
AUR	1.956	.000
CDR	4.164	.000
CER	2.961	.000
DDR	78.987	.000
DER	22.832	.000
HDR	2.960	.000
HER	2.207	.000
LDR	1.003	.000
LER	.702	.000
LTDR	1.706	.000
LTER	1.455	.000
LCDR	1.706	.000
LCER	1.455	.000
LNDR	1.756	.000
LNER	1.505	.000
LPDR	1.756	.000
LPER	1.505	.000
MDR	27.149	.000
MER	11.943	.000
SDR	4.165	.000
SER	3.011	.000
SER	3.010	.000
SER	3.010	.000

Table 6-8. Floating Point Register - Register Operands (cont)

Operand	Inst Time	IBM Spec
SWR	3.462	.000
SUR	2.458	.000
AXR	7.728	.000
LRDR	1.254	.000
LRER	1.003	.000
MXR	116.474	.000
SXR	10.638	.000

Table 6-9. Floating Point Register
Indexed Storage Operands Without Indexing

Operand	Inst Time	IBM Spec
AD	4.567	.000
AE	3.463	.000
AW	3.814	.000
AU	2.710	.000
CD	4.818	.000
CE	3.714	.000
DD	79.941	.000
DE	23.887	.000
LD	1.606	.000
LE	1.404	.000
MD	3.663	.000
ME	3.663	.000
STD	2.157	.000
STE	1.455	.000
SD	4.919	.000
SE	3.864	.000

Table 6-9. Floating Point Register
Indexed Storage Operands Without Indexing (cont)

Operand	Inst Time	IBM Spec
SW	4.115	.000
SU	3.212	.000
MXD	36.081	.000

Table 6-10. Floating Point Register
Indexed Storage Operands With Indexing

Operand	Inst Time	IBM Spec
AD	4.767	.000
AD	4.767	.000
AE	3.664	.000
AW	4.015	.000
AU	2.911	.000
CD	5.019	.000
CE	3.915	.000
DD	80.142	.000
DE	24.087	.000
LD	1.807	.000
LE	1.606	.000
MD	3.863	.000
ME	3.863	.000
STD	2.358	.000
STE	1.656	.000
SD	5.119	.000
SE	4.065	.000
SW	4.317	.000
SU	3.413	.000
MXD	36.282	.000

Table 6-11. Storage Implied - Register Operands

Operation	Operand	Inst Time	IBM Spec
Test and Set	TS	3.060	.000
Store Clock	STCK	5.718	.000
Store Clock Comparator	STCKC	4.265	.000
Store CPU Timer	STPT	5.165	.000
Set Clock Comparator	SCKC	8.600	.000
Purge TLB	PTLB	12.001	.000
Reset Reference Bit	RRB	2.508	.000
Start I/O - Device FFF	SIO	3.111	.000
Start I/O Fast Rlse - Dev FFF	SIOF	3.111	.000
Store Channel ID - Chan 0	STIDC	5.119	.000
Store Channel ID - Chan 1	STIDC	5.119	.000
Store CPU ID	STIDP	3.763	.000
Test Channel - Chan 0	TCH	4.416	.000
Test Channel - Chan 1	TCH	4.416	.000
Test I/O - Device 000	TIO	10.338	.000
Test I/O - Device 01F	TIO	16.461	.000
Clear I/O - Device 000	CLRIO	10.338	.000
Clear I/O - Device 01F	CLRIO	16.461	.000
Halt Device - Device 000	HDV	10.539	.000
Halt Device - Device 01F	HDV	13.299	.000
Halt I/O - Device 000	HIO	10.539	.000
Halt I/O - Device 01F	HIO	13.299	.000
Set Clock (Disabled)	SCK	3.312	.000
Set CPU Timer	SPT	4.459	.000
Set System Mask - Suppress Off	SSM	5.169	.000
Set System Mask - Suppress On	SSM	247.003	.000
Load PSW	LPSW	5.671	.000
Insert PSW Key	IPK	2.208	.000
Set PSW Key From Address	SPKA	3.211	.000

APPENDIX A

ABBREVIATIONS

Appendix A. Abbreviations

ACR	Automatic Carriage Return
A/D	Alter/Display
ALT	Alternate
ASCII	American Standard Code Information Interchange
BC	Basic Control
CC	Condition Code
CCH	Channel Check Handle
CCW	Channel Control Word
CHAN	Channel
CHAR	Character
CIDA	Channel-Indirect-Data-Addressing
CLK	Clock
CPU	Central Processor Unit
CSW	Channel Status Word
CTRL	Control
DASF	Direct Access Storage Facility
DAT	Dynamic Address Translation
DOS	Disk Operating System
DSF	Disk Storage Facility
EBCDIC	Extended Binary Coded Decimal Interchange Code
EC	Extended Control
ECC	Error Checking and Corrections
ECSW	Extended Channel Status Word
EOB	End of Block
HDX	Hexadecimal
IBM	International Business Machines

ID	Identification
IDA	Indirect-Data-Address
IDAL	Indirect-Data-Address-List
IDALW	Indirect-Data-Address-List-Word
IL	Incorrect Length
ILC	Instruction Length Code
IMPL	Initial Microprogram Load
I/O	Input/Output
K	Key
LF	Left
LOC	Local
M	Machine
MM	Millimeter
NL	New Line
NO-OP	No-Operation
OS	Operating System
P	Problem
PER	Program Event Recorder
PM	Program Mask
PR-KB	Printer-Keyboard
PSW	Program Status Word
REG	Register
SEL	Select
SIO	Start I/O
SLI	Suppress Length Indicator
ST	Store Status
STD	Standard
T	Timer

TIC	Transfer In Channel
TLB	Translator-Lookaside-Buffer
TOD	Time Of Day
UCW	Unit Control Word
VM	Virtual Memory
VMA	Virtual Machine Assist
VS	Virtual System
W	Wait

COMMENT SHEET

MANUAL TITLE CDC® OMEGA/480 Model 1 Functional Characteristics

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